

64Mb SDRAM

- 3.3 volt 4Mx16
- 125/133/143/166/183/200 MHz SDRAM
- 4 banks, 4K refresh

GENERAL DESCRIPTION

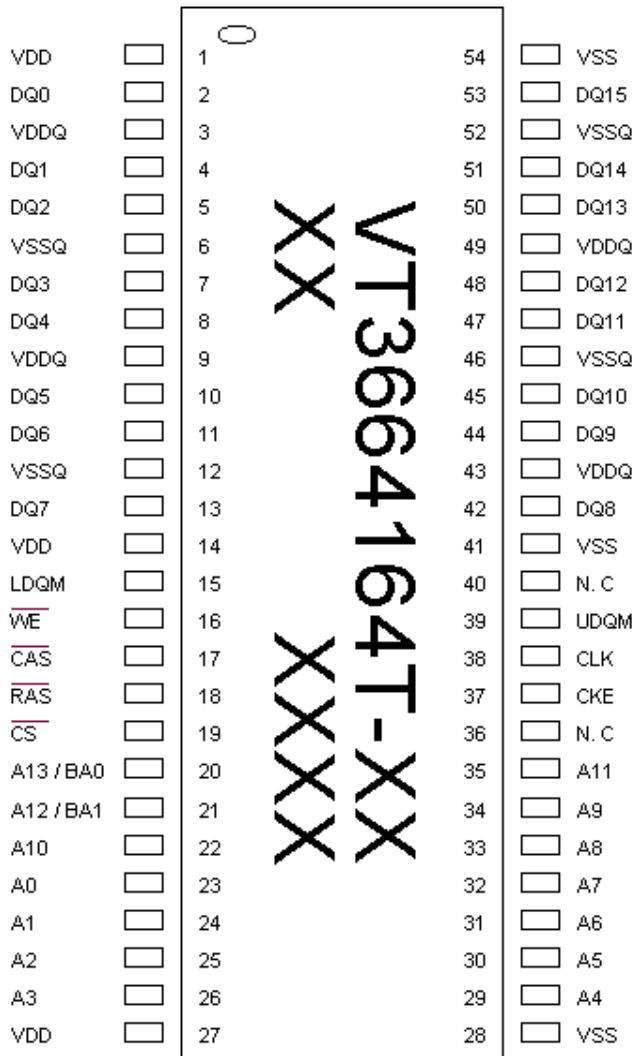
The VT3664164T is a high-speed synchronous dynamic random access memory (SDRAM), organized as 1M words x 4 banks x 16 bits. Using pipelined architecture technology. Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1,2,4,8 or full page when a bank and row is selected by an ACTIVE command. By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance.

FEATURES

- 3.3V \pm 0.3V power supply
- 1,048,576 words x 4 banks x 16 bits organization
- Four banks operation
- Power-down Mode
- Sequential and interleave burst
- Burst Length: 1,2,4,8 and full page
- CAS latency: 2 and 3
- 4K refresh cycles/64 ms
- Auto & self refresh
- DQM for masking
- Burst read single-bit write operation
- LVTTTL compatible with multiplexed address
- All inputs are sample at the positive going edge of the system clock
- Reflow temperature condition: Max 245°C ~250°C
- The environmental testing temperature :
All type of VT SDRAM testing temperature at 75°C (Max).

PIN CONFIGURATION (Top view)

54-Pin Plastic TSOP (II) (400mil)



AVAILABLE PART NUMBER

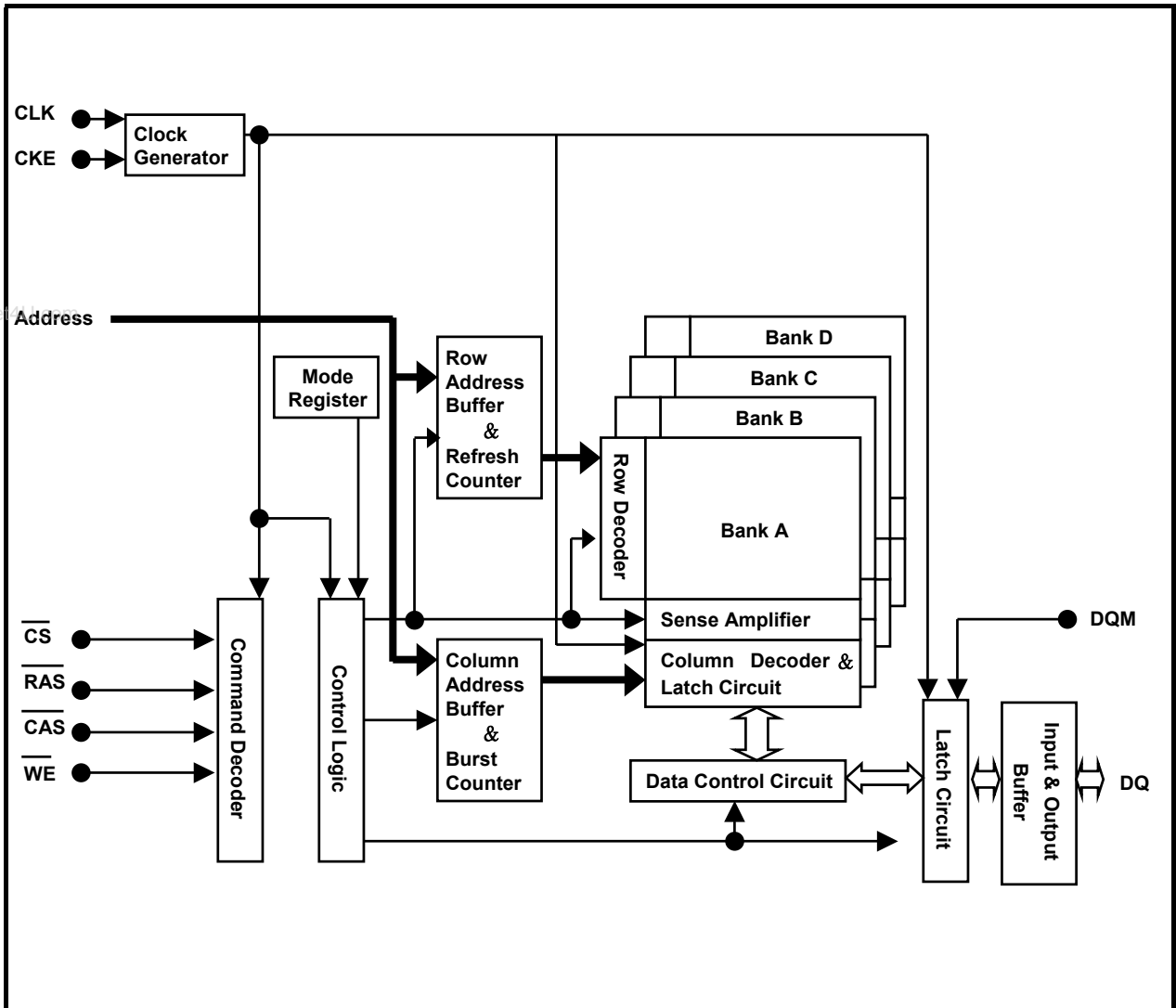
PART NUMBER	SPEED
VT3664164T-7	125MHz
VT3664164T-7H	133MHz
VT3664164T-6L	143MHz
VT3664164T-6	166MHz
VT3664164T-5L	183MHz
VT3664164T-5	200MHz

Note : The second row (xx xxxx) part number is kreton's product serial number and data code.

PIN DESCRIPTION

PIN NAME	FUNCTION	DESCRIPTION
A ₀ - A ₁₁	Address	Multiplexed pins for row and column address. Row address: A ₀ -A ₁₁ . Column address: A ₀ -A ₇ .
BA ₀ - BA ₁	Bank Select	Select bank to activate during row address latch time, or bank to read/write during address latch time.
DQ ₀ - DQ ₁₅	Data Input / Output	Multiplexed pins for data output and input.
/CS	Chip Select	Disable or enable the command decoder.
/RAS	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with /RAS low.
/CAS	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with /CAS low.
/WE	Write Enable	Enables write operation and row precharge.
DQM	Input/output mask	Makes data output Hi-z. Blocks data input when DQM active.
CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode or Self Refresh
V _{DD}	Power (+3.3V)	Power for input buffers and logic circuit inside DRAM.
V _{SS}	Ground	Ground for input buffers and logic circuit inside DRAM.
V _{DDQ}	Power (+3.3V) for I/O buffer	Separated power from V _{DD} , to improve DQ noise immunity.
V _{SSQ}	Ground for I/O buffer	Separated power from V _{SS} , to improve DQ noise immunity.
NC	No Connection	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.3 to +3.6	V
Supply voltage relative to V_{SS}	V_{DD}, V_{DDQ}	-0.3 to +3.6	V
Short circuit current	I_{OS}	50	mA
Power dissipation	PD	1.0	W
Operating temperature	T_{OPT}	0 to +60	°C
Storage temperature	T_{STG}	-55 to +125	°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended DC operating conditions (Voltage referenced to $V_{SS} = 0V$, $T_A = 0$ to $70^{\circ}C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0		$V_{DD}+0.3$	V	
Input low voltage	V_{IL}	-0.3		0.8	V	

CAPACITANCE ($V_{DD}=3.3V$, $T_A=25^{\circ}C$, $f=1MHz$, $V_{REF}=1.4V+200mV$)

PARAMETER	SYMBOL	TYP	MAX	UNIT
Input capacitance ($A_0 - A_{10}, BS$)	C_{IN1}	2.5	5	Pf
Input capacitance ($/RAS, /CAS, /WE$)	C_{IN2}	2.5	5	Pf
Input capacitance (CKE)	C_{IN3}	2.5	5	Pf
Input capacitance (CLK)	C_{IN4}	2.5	5	Pf
Input capacitance ($/CS$)	C_{IN5}	2.5	5	Pf
Input capacitance (DQM)	C_{IN6}	2.5	5	Pf
Data input/output capacitance ($DQ_0 - DQ_{15}$)	$C_{I/O}$	4.0	6.5	Pf

TABLE OF OPERATING MODES

COMMAND TRUTH TABLE

FUNCTION	SYMBOL	CKE		/CS	/RAS	/CAS	/WE	BA	A10	A9 - A0
		n-1	N							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X
CBR (Auto) refresh	REF	H	H	L	L	L	H	X	X	X
Self refresh	SELF	H	L	L	L	L	H	X	X	X
Data mask/output disable	MASK	H	X	X	X	X	X	X	X	X
Clock suspend mode entry		H	L	X	X	X	X	X	X	X
Clock suspend		L	L	X	X	X	X	X	X	X
Clock suspend mode exit		L	H	X	X	X	X	X	X	X
Power down entry		H	L	X	X	X	X	X	X	X
Power down exit		L	H	X	X	X	X	X	X	X

H:High level, L:Low level

X:High or Low level (Don't care), V: Valid Data input

AC CHARACTERISTICS AND OPERATING CONDITION

(V_{CC}=3.3V±0.3V, Ta=0° to 70°C)

SYMBOL	PARAMETER	-5 (200MHz)		-5L (183MHz)		-6 (166MHz)		-6L (143MHz)		-7H (133MHz)		-7 (125MHz)		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Ref/Active to Ref/Active Command Period	54		55		60		63		67.5		70		ns
t _{RAS}	Active to precharge Command Period	40	100K	38.5	100K	42	100K	42	100K	45	100K	50	100K	
t _{RCD}	Active to Read/Write Command Delay Time	14		16.5		18		20		20		20		
t _{CCD}	Read/Write(a) to Read/Write(b) Command	1		1		1		1		1		1		cycle
t _{RP}	Precharge to Active(b) Command Period	14		15		15		20		20		20		ns
t _{RRD}	Active(a) to Active(b) Command Period	10		11		12		14		15		20		
t _{CK}	CLK Cycle Time	5		5.5		6		7		7.5		8		
t _{CH}	CLK High Level	2		2.3		2.5		2.5		2.5		3		
t _{CL}	CLK Low Level	2		2.3		2.5		2.5		2.5		3		
t _{AC}	Access Time from CLK		5.5		5		5		5.4		5.4		6	
t _{OH}	Output Data Hold Time	2		2		2.5		2.7		2.7		3		
t _{HZ}	Output Data High Impedance Time	2	5	2	5	2.5	5	2.7	5.4	2.7	5.4	3	6	
t _{LZ}	Output Data Low Impedance Time	0		0		0		0		0		0		
t _T	Transition Time of CLK(Rise and Fall)	1	10	1	10	1	10	1	10	1	10	1	10	
t _{DS}	Data-in-Set-up Time	1.5		1.5		1.5		1.5		1.5		2		
t _{DH}	Data-in Hold Time	0.8		0.8		0.8		0.8		0.8		1		
t _{AS}	Address Set-up Time	1.5		1.5		1.5		1.5		1.5		2		
t _{AH}	Address Hold Time	0.8		0.8		0.8		0.8		0.8		1		
t _{CKS}	CKE Set-up Time	1.5		1.5		1.5		1.5		1.5		2		
t _{CKH}	CKE Hold Time	0.8		0.8		0.8		0.8		0.8		1		
t _{CMS}	Command Set-up Time	1.5		1.5		1.5		1.5		1.5		2		
t _{CMH}	Command Hold Time	0.8		0.8		0.8		0.8		0.8		1		
t _{REF}	Refresh Time		64		64		64		64		64		64	ms
t _{RSC}	Mode Register Set Cycle Time	2		2		2		2		2		2		CLK
t _{DPL}	Data in to Precharge	1		1		1		1		1		1		
t _{SB}	Power Down Mode Entry Time	1		1		1		1		1		1		
t _{BDL}	Last Data in to Burst Stop	1		1		1		1		1		1		
t _{DAL}	Data in to Active Command	t _{DPL} +		t _{DPL} +		t _{DPL} +		t _{DPL} +		t _{DPL} +		t _{DPL} +		

(CL=CAS Latency)

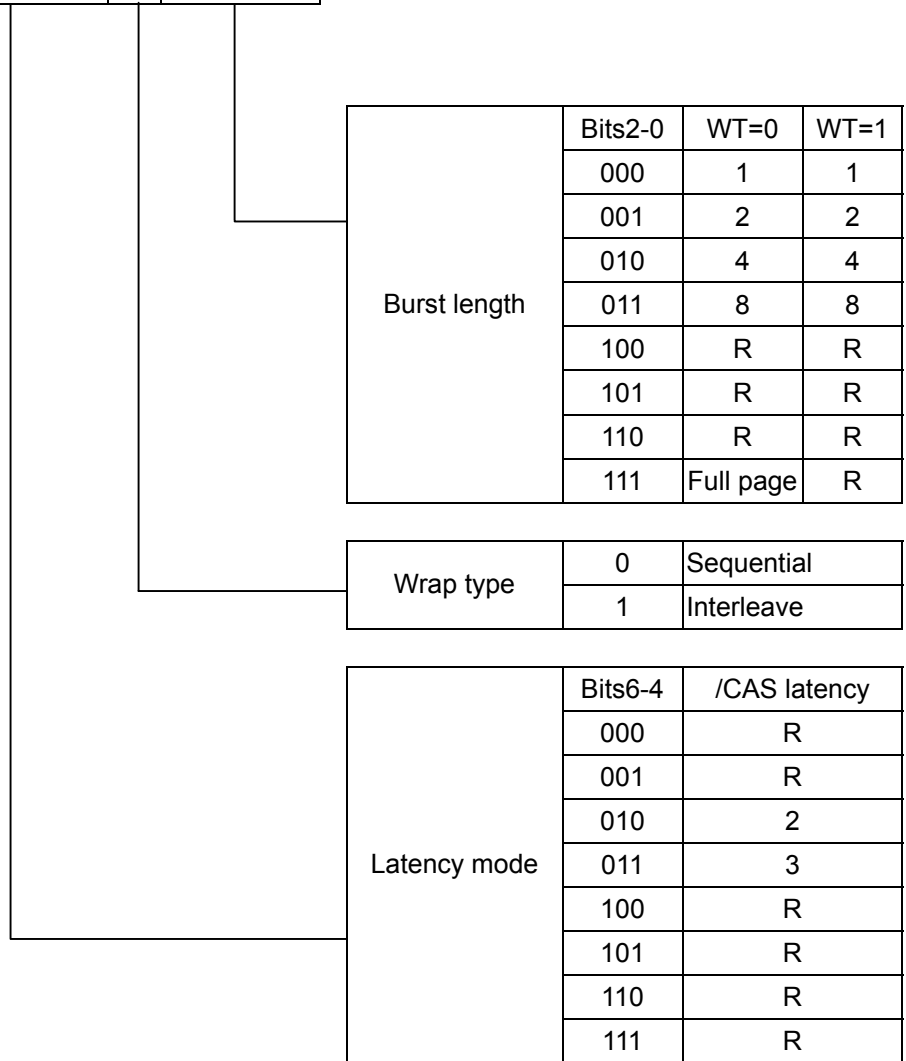
MODE REGISTER (ADDRESS INPUT FOR MODE SET)

11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	1	Reserved						JEDEC Standard test Set	

11	10	9	8	7	6	5	4	3	2	1	0	
x	x	1	0	0	LTMODE	WT	BL					Burst Read and Single Write (for Write Through Cache)

11	10	9	8	7	6	5	4	3	2	1	0	
x	x	0	0	0	LTMODE	WT	BL					Burst Read and Burst Write X=Don't care

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Burst length	Bits2-0	WT=0	WT=1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
111	Full page	R	

Wrap type	0	Sequential
	1	Interleave

Latency mode	Bits6-4	/CAS latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
111	R	

Remark R: Reserved

DC CHARACTERISTICS

 Recommended D.C. Operating condition ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

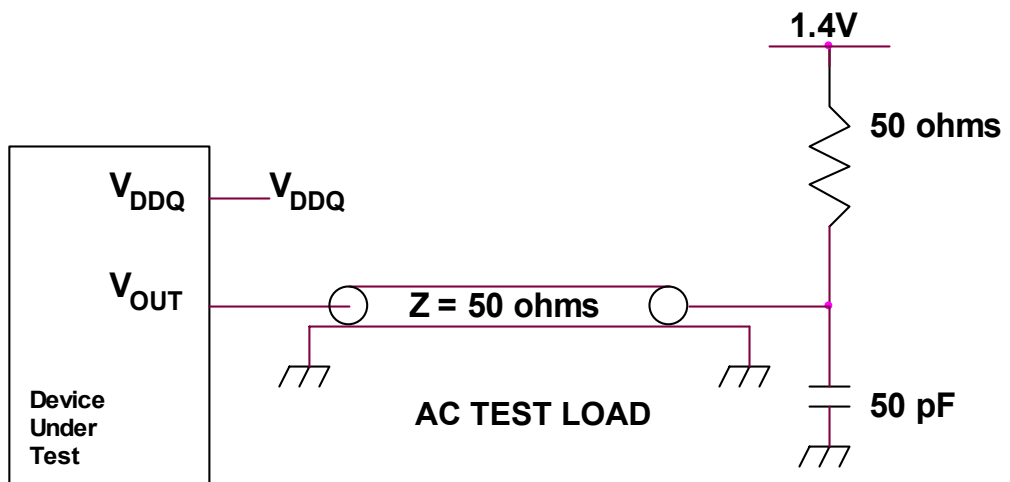
DESCRIPTION/TEST CONDITION	SYMBOL	-5		-5L		-6		-6L		-7H		-7		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current $t_{RC} \geq t_{RC(min)}$, Outputs Open Address changed once during $t_{CK(min)}$. Burst Length = 1 (One Bank Active)	I_{CC1}		110		100		95		85		85		80	mA
Precharge Standby Current in non power-down mode $t_{CK} = t_{CK(min)}$, $/CS \geq V_{IH(min)}$, $CKE \geq V_{IH(min)}$, Input signals are changed once during 30ns.	I_{CC2N}		20		20		20		20		20		20	
Precharge Standby Current in non power-down mode $t_{CK} = \infty$, $CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, Input signals are stable	I_{CC2NS}		20		20		20		20		20		20	
Precharge Standby Current in power-down mode $t_{CK} = t_{CK(min)}$, $CKE \leq V_{IL(max)}$	I_{CC2P}		2		2		2		2		2		2	
Precharge Standby Current in power-down mode $t_{CK} = \infty$, $CKE \leq V_{IL(max)}$, $CLK \leq V_{IL(max)}$	I_{CC2PS}		1		1		1		1		1		1	
Active Standby Current in non power-down mode $CKE \geq V_{IH(min)}$, $t_{CK} = t_{CK(min)}$ (Both Bank Active)	I_{CC3N}		35		35		35		35		35		35	
Active Standby Current in power-down mode $CKE \leq V_{IL(max)}$, $t_{CK} = t_{CK(min)}$, $/CS \geq V_{IH(min)}$ (Both Bank Active)	I_{CC3P}		7		7		7		7		7		7	
Operating Current (Page Burst, and All Bank activated) $t_{CCD} = t_{CCD(min)}$, Outputs Open, Multi-bank interleave, gapless data	I_{CC4}		150		140		130		100		100		80	
Refresh Current $t_{RC} \geq t_{RC(min)}$, ($t_{REF} = 32ms$)	I_{CC5}		170		160		150		130		130		110	
Self Refresh Current $CKE \leq 0.2V$	I_{CC6}		0.5		0.5		0.5		0.5		0.5		0.5	

LEAKAGE AND OUTPUT BUFFER CHARACTERISTICS

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current ($0V \leq V_{IN} \leq V_{DD}$ All other pins not under test = 0V)	-5	5	μA
I_{OL}	Output Leakage Current Output disable, ($0V \leq V_{OUT} \leq V_{DDQ}$)	-5	5	μA
V_{OH}	LVTTL Output "H" Level Voltage ($I_{OUT} = -2mA$)	2.4	-	V
V_{OL}	LVTTL Output "L" Level Voltage ($I_{OUT} = 2mA$)	-	0.4	V

PARAMETER	CONDITIONS
AC input Levels (V_{IH}/V_{IL})	2.0/0.8V
Input rise and fall time	1ns
Input timing reference level/ Output timing reference level	1.4V
Output load condition	50pF

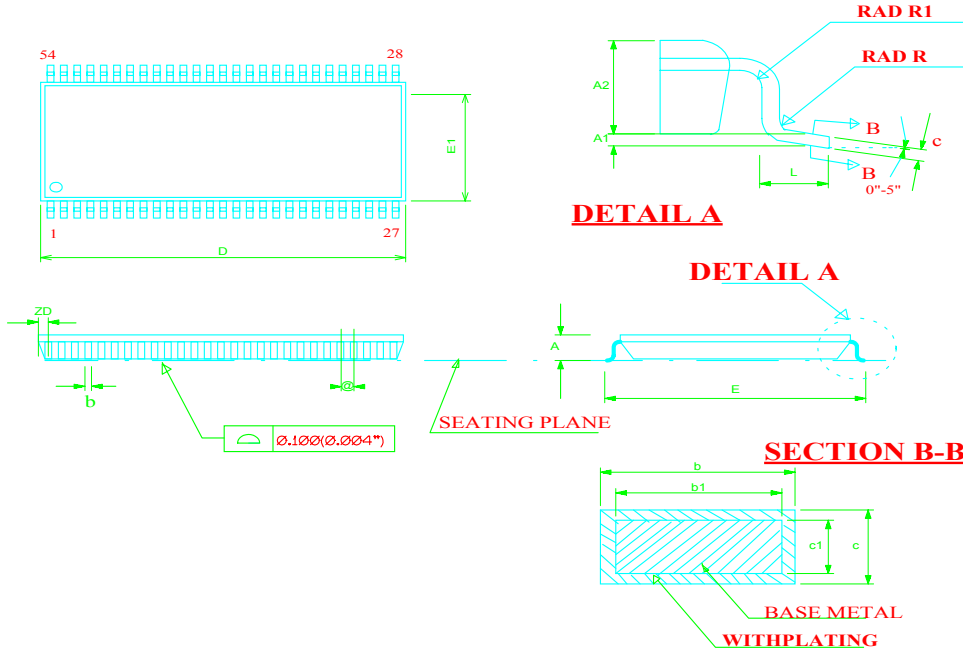
AC Test Load Circuits (for LVTTTL interface) :



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PACKAGING INFORMATION

■ 400mil, 54-pin Plastic TSOP



DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.20	0.047
A1	0.05	...	0.15	0.002	...	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	...	0.45	0.012	...	0.018
b1	0.30	...	0.40	0.012	...	0.016
c	0.12	...	0.21	0.005	...	0.008
c1	0.12	...	0.16	0.005	...	0.006
D	22.09	22.22	22.35	0.870	0.875	0.880
ZD	0.71 REF			0.028 REF		
@	0.80 BASIC			0.0315 BASIC		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
R	0.12	...	0.25	0.005	...	0.010
R1	0.12	0.005

NOTE:

- 1 - CONTROLLING DIMENSION: MILLIMETERS
- 2 - DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15mm(0.006") PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION. INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25mm(0.01") PER SIDE.
- 3 - DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS / INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm. DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.