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INPUT/OUTPUT DESCRIPTION: (continued) OUTPUTS 06, 05, 04 (PINS 3-5).

These outputs provide the base current (through external limiting resistors) to NPN drivers of the motor coils. They are enabled in the sequence described in Table 1 and for a duration as determined by the internal speed regulation data.

OUTPUTS 03, 02, 01 (PINS 6-8).

The outputs provide the base current to the PNP drivers of the motor coils. They are enabled per Table 1 and the internal speed regulation data.

DESCRIPTION OF OUTPUT SIGNALS: (See Figures 2C, 3C)

An output pair turn on at a change of commutator input state and remain on for a period of time determined by the rotational speed measured within the latest sampling window. The output pulse can be zero if speed is too high. If other than zero, the output width follows the formula OpW (Clock Periods) = $(192 + n \times 384) \times 4 \div$ number of poles, where n varies from zero to 14. If the look up table indicates n is greater than 14, the pair remain on until the next commutation change.

VSS (PIN 9).

Supply voltage positive terminal, (+10 to +28 Vdc.) A, B, C INPUTS (PINS 10-12).

These inputs have pull up resistors and provide control of the output commutation sequence as per Table 1. A, B, C orginate at the position sensors of the motor (see fig. 2) and must sequence in cyclic order (only one input changes at any time). Figure C illustrates a method for controlling the motor direction of rotation. Figure D indicates how one external invertor may be used to use a 120° circuit type in a 60° sensor separation application (or 60° to 120°).

OSC IN (PIN 13), OSC OUT (PIN 14)

Pin 13 provides one of the two ports necessary for connecting a crystal. It may also be used to drive the circuit from an external clock. Pin 14 is used as the second connection when using a crystal for oscillation. Limited variable speed operation can be obtained by using the oscillator depicted in Figure A whose nominal frequency is 3.58 MHz.

FREQUENCY TEST POINT (PIN 15).

This test output provides the user with a point to measure the oscillator frequency without loading the oscillator. It provides a signal which is one sixth of the oscillator frequency.

VDD (PIN 16).

Supply voltage negative terminal (ground).

OVERCURRENT DETECT (PIN 17).

The Overcurrent Detection Input provides the user a way of protecting the motor windings, drivers and power supply from an overload condition. The user provides a fractional ohm resistor between the positive supply and the common emitters of the PNP drivers. This point is connected to a potentiometer (e.g. 100k ohm), the other end of which is connected to around and the wiper connected to the overcurrent input. The wiper pickoff is adjusted so that the outputs 0_1 - 0_6 are off for currents greater than the limit. (Reference Fig. 5) An alternative overcurrent detection circuit is illustrated in Figure B. An overcurrent condition is sensed and latched causing the overcurrent input (pin 17) to become low. When the overcurrent condition terminates, the next positive edge of the chopping frequency will cause pin 17 to become high. This circuit limits the maximum output switching rate to the chopping frequency when an overcurrent condition occurs.

An example of setting up the over current follows:

- Determine the fractional ohm resistance and the maximum current to determine the voltage drop across the resistor and call this V_{OC}.
- 2. Apply V_{SS} - V_{OC} to the fractional ohmage end of the potentiometer.
- 3. Hold A, B and C in a known state (e.g. 000). This will enable a pair of outputs in accordance with Table 1.
- 4. Adjust the potentiometer until outputs 0_1 - 0_3 are all at V_{SS} and 0_4 - 0_6 are at ground.
- 5. Remove the voltage from the potentiometer and connect the potentiometer to the transistor end of the fractional ohm resistor.

TACHOMETER INPUT (PIN 18).

The signal applied to the tachometer input originates at a motor position sensor (one of the commutation inputs may be used). Each negative edge of the tachometer input is synchronized by the one sixth oscillator frequency. The resulting signal 1) transfers new speed regulation data to the "on time" data storage latches, 2) resets the clock pulse accumulator and 3) originates a new sampling window. The tachometer input is provided with a pull-up resistor.

MAXIMUM RATINGS:

| PARAMETER | SYMBOL | VALUE | UNITS | |
|---------------------------------------|--------------------------------------|---------------------|-----------|-------|
| Storage Temperature | T _{stg} | -65 to +150 | °C | |
| Operating Temperature | - | | _ | |
| 1. Plastic | T _{ap} | -25 to +70 | °C | |
| 2. Ceramic | Tac | -55 to +125 | <u> </u> | |
| Voltage (any pin to V _{SS}) | Vmax | -30 to $+ 0.5$ | VOLTS | |
| DC ELECTRICAL CHARACTER | STICS: $(+10 \text{ to } +2)$ | 8 VDC) | | |
| SUPPLY CURRENT | SYMBOL | MIN. | MAX. | UNITS |
| (Excluding Outputs) | lop | | 22 | mA |
| | UU | | 22 | IIIA |
| INPUT SPECIFICATIONS: | | | | |
| Brake, commuting and tachon | neter (Pins 2, 10, 11, | 12, 18) | | |
| INPUT VOLTAGE | MIN. | MAX. | UNITS | |
| Logic ''1'' | V _{SS} - 2.5 | V _{SS} | VOLTS | |
| Logic ''0'' | 0 | V _{SS} - 5 | VOLTS | |
| - | | | | |
| INDUT CURRENT | | | | |

INPUT CURRENT

Each of the five inputs provides an internal constant current source to V_{SS} of 200 to 400ua (typically 300ua)

| VERCURRENT DETECTION INPUT (PIN 17) | 11 | NPU | TS | TABL Output s | E 1A –01, Driver | DRIVER | DRIVER |
|--|---|-----------------------------------|------------------------------------|--|---|---|---------------------------------------|
| NPUT VOLTAGE MIN. MAX. UNITS | A | B | Ċ | ENABLED | A* | B * | C+ |
| ogic ''1'' $(V_{SS} \div 2) + .25$ V_{SS} VOLTS | 0 | 0 | 0 | 01, 05 | + | - | OFF |
| ogic ''0'' 0 $(V_{SS} \div 2)25$ VOLTS | 1 | Õ | 0 | 03, 05 | OFF | _ | + |
| heroretical switching point for the Overcurrent Detection Input | 1 | 1 | | 03, 04 | - | OFF | + |
| one half of the power supply. Manufacturing tolerances cause | 1 | 1 | | $0_2, 0_4$ | _ | + | OFF |
| e switching point to vary plus or minus .25 volts. After man- | 0 | 1 | 1 | 0 ₂ , 0 ₆ | OFF | + | - |
| cture, the switching point remains within 10mv over time difference of the second second second second second s | 0 | 0 | 1 | 01, 06 | + | OFF | - |
| DmV. There is no hysteresis on the overcurrent detection input. | | | | TABLE 1 | B -02, -03 | | |
| SCILLATOR INPUT (PIN 13). (When driven from external | | NPU | ITS | OUTPUT S | DRIVER | DRIVER | DRIVER |
| urce.) | A | B | C | ENABLED | A* | B* | C* |
| MIN. MAX. UNITS | 0 | 0 | 1 | 0 ₂ , 0 ₆ | OFF | + | - |
| aic ''1'' V _{SS} —1 V _{SS} VOLTS | 1 | Õ | 1 | $0_2, 0_4$ | - | + | OFF |
| gic ''0'' 0 V _{SS} -6 VOLTS | 1 | | 0 | 0 ₃ , 0 ₄ | - | OFF | + |
| UTPUT SPECIFICATIONS | 1 | | 0 | 0 ₃ , 0 ₅ | OFF | | + |
| | 0 | | 0 | $0_1, 0_5$ | + | _ OFF | OFF |
| 6 KHz TEST (PIN 15) signed for 10MΩ , 20pf scope probe. | 0 Pue | 1 sh r | 1 1 | 0 ₁ , 0 ₆ drivers are ma | · | - | |
| S DETECT OUTPUT (PIN 1) | (Dr | iver | · A), | 0 ₂ and 0 ₅ (Drive | er B), O_3 and | 0 ₆ (Driver C |). |
| MIN. MAX. UNITS CONDITIONS OURCE 1.0 mA Output short circuit to V _{DD} | *Se | e ⊦ | ig. 4 | | | | |
| INK 10.0 ua Output at .5V | | | | DESCRIPTIO | N OF AVAILA | BLE TYPES | |
| 1-0 ₆ (PINS 3-8) | | | | | SEN | | |
| 1-03 are current sinks | Ι ΤΥΙ | PE | | POLES | SEPAR | ATION | GAIN* |
| | 726 | 63-(|)1 | 4 | 6 | 0° | Medium |
| -O ₆ are current sources | • | 63-(| | 8 | 12 | 0° | High |
| 5 | 1 1 | | | 4 | 12 | | Medium |
| tputs turn on in pairs (see figs. 2C, 3C and 4). For example | 726 | | | 8 | 12 | 0° | Mediun |
| tputs turn on in pairs (see figs. 2C, 3C and 4). For example ee dotted line, fig. 4): and Q4 are on, thus enabling a path from the positive supply rough the fractional ohm resistor, emitter-base junction of | 726 | 63-(|)7 | U | | | |
| utputs turn on in pairs (see figs. 2C, 3C and 4). For example ee dotted line, fig. 4): 8 and Q4 are on, thus enabling a path from the positive supply rough the fractional ohm resistor, emitter-base junction of 101, Q8, Q4, R5 and the base emitter junction of Q105 to round. The current in the above described pattern is determined | 726 726 *Ga | 63-(in d | escr | ibes the change | of output du | ity cycle as type, the d | a function Juty cycle |
| utputs turn on in pairs (see figs. 2C, 3C and 4). For example see dotted line, fig. 4): 8 and Q4 are on, thus enabling a path from the positive supply rough the fractional ohm resistor, emitter-base junction of 101, Q8, Q4, R5 and the base emitter junction of Q105 to round. The current in the above described pattern is determined y the power supply voltage, the value of R1, the voltage drops cross the base-emitter, junction of Q101 and Q105 (1.4 volts for | 726 726 *Ga chai caus | 63-(in d nge sed | escr mot | ibes the change tor speed. For t hange from 0% | he high gain to 100% ove | type, the c er a 6 RPM | luty cycle motor spe |
| utputs turn on in pairs (see figs. 2C, 3C and 4). For example see dotted line, fig. 4): 8 and Q4 are on, thus enabling a path from the positive supply brough the fractional ohm resistor, emitter-base junction of 101, Q8, Q4, R5 and the base emitter junction of Q105 to round. The current in the above described pattern is determined y the power supply voltage, the value of R1, the voltage drops cross the base-emitter, junction of Q101 and Q105 (1.4 volts for ingle transistor or 2.8V for Darlington pairs), the impedance of | 726 726 *Ga chai caus chai | 63-(in d nge sed nae | escr mot to c For | ibes the change tor speed. For t | the high gain to 100% ove tin type, the (| type, the c er a 6 RPM duty cycle c | luty cycle motor spe hanges fro |
| A-O ₆ are current sources Dutputs turn on in pairs (see figs. 2C, 3C and 4). For example see dotted line, fig. 4): A8 and Q4 are on, thus enabling a path from the positive supply hrough the fractional ohm resistor, emitter-base junction of Q101, Q8, Q4, R5 and the base emitter junction of Q105 to pround. The current in the above described pattern is determined by the power supply voltage, the value of R1, the voltage drops icross the base-emitter, junction of Q101 and Q105 (1.4 volts for single transistor or 2.8V for Darlington pairs), the impedance of D8 and Q4 and the value of R5. | 726 726 *Ga chai caus chai 0% | in d nge sed nge to | escr mot to c For 1009 | ibes the change tor speed. For t hange from 0% the medium ga % when the mo | the high gain to 100% ove tin type, the (| type, the c er a 6 RPM duty cycle c | luty cycle motor spe hanges fro |

| POWER SUPPLY VOLTS | 20 | 15 | 10 | 7.5 | 5 | 2.5 | mA |
|--------------------------|-----|-----|-----|-----|-----|-----|----|
| 12 | | .25 | .56 | .86 | 1.5 | 3.3 | |
| 15 | .33 | .51 | .92 | 1.3 | 2.1 | 4.6 | |
| 18 | * | .76 | 1.3 | 1.7 | 2.8 | 5.8 | |
| 21 | | * | 1.6 | 2.2 | 3.3 | 7.0 | |
| 24 | • | * | 1.9 | 2.6 | 4.0 | 8.3 | |
| 28 | * | * | * | 3.2 | 4.9 | 9.9 | |

*causes excessive power dissipation.

RESISTANCE IN KILOHMS

LS7263



LSI/CSI 4





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