# PMV65XP

## P-channel TrenchMOS™ extremely low level FET

Rev. 01 — 28 September 2004 Product data sheet

## 1. Product profile

### 1.1 General description

P-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Low threshold voltage
- Low on-state resistance.

### 1.3 Applications

- Low power DC-to-DC converters
- Load switching
- Battery management
- Battery powered portable equipment.

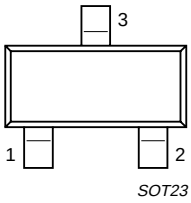
### 1.4 Quick reference data

- $V_{DS} \leq -20$ V
- $R_{DSon} \leq 76$ mΩ
- $I_D \leq -3.9$ A
- $Q_{gd} = 0.65$ nC (typ).

## 2. Pinning information

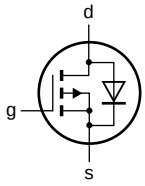
**Table 1: Discrete pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | gate (g) | | |
| 2 | source (s) | | |
| 3 | drain (d) | | |




SOT23

**SOT23**

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## 3. Ordering information

**Table 2: Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PMV65XP | SOT23 | Plastic surface mounted package; 3 leads | SOT23 |

## 4. Limiting values

**Table 3: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C | - | –20 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | - | –20 | V |
| $V_{GS}$ | gate-source voltage (DC) | | - | ±12 | V |
| $I_D$ | drain current (DC) | $T_{sp}$ = 25 °C; $V_{GS}$ = –4.5 V; Figure 2 and 3 | - | –3.9 | A |
| | | $T_{sp}$ = 100 °C; $V_{GS}$ = –4.5 V; Figure 2 | - | –2.5 | A |
| $I_{DM}$ | peak drain current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; Figure 3 | - | –15.9 | A |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C; Figure 1 | - | 1.92 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –55 | +150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source (diode forward) current (DC) | $T_{sp}$ = 25 °C | - | –1.6 | A |
| $I_{SM}$ | peak source (diode forward) current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs | - | –6.4 | A |


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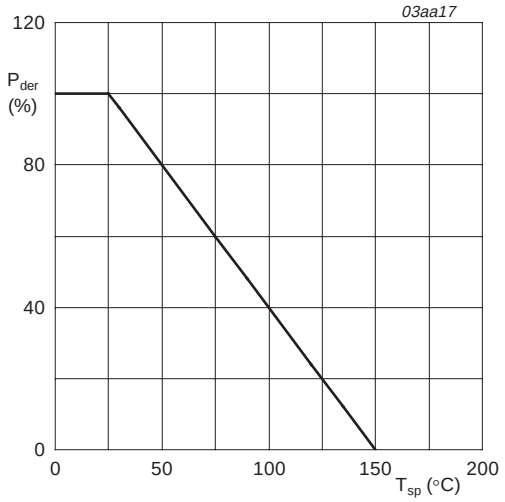
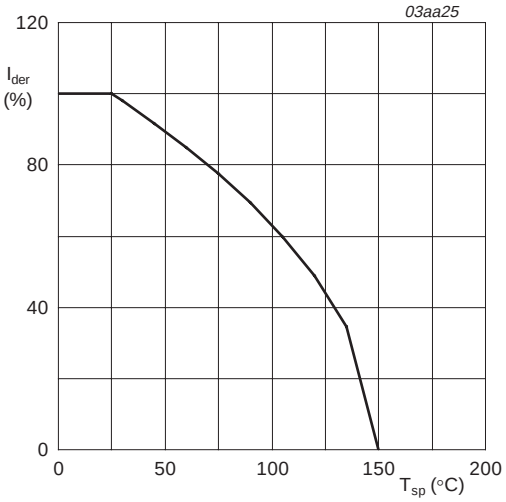


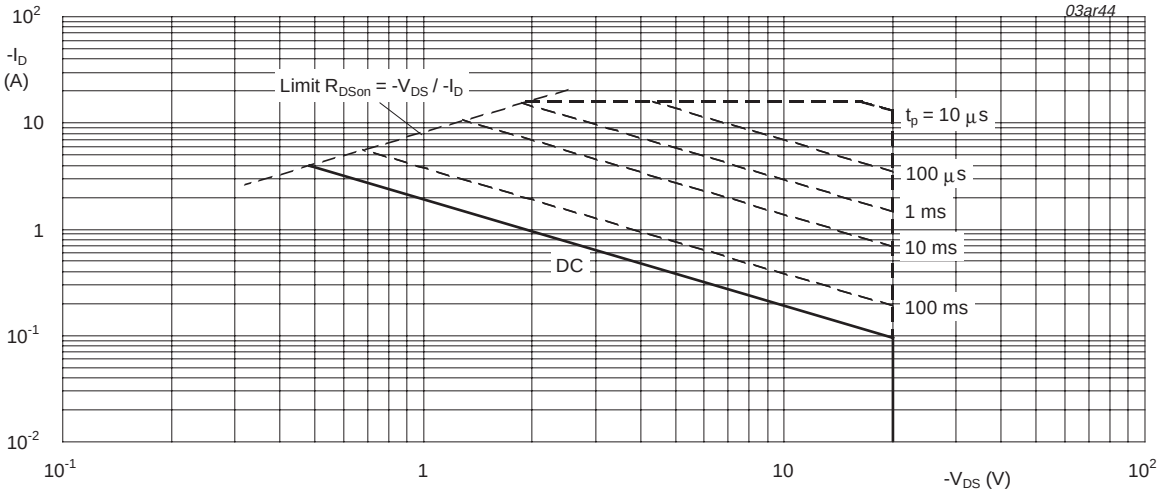

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of solder point temperature.**




$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of solder point temperature.**




$T_{sp}$ = 25 °C; $I_{DM}$ is single pulse; $V_{GS}$ = –4.5 V

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**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# 5. Thermal characteristics

**Table 4: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}sp)}$ | thermal resistance from junction to solder point | Figure 4 | - | - | 65 | K/W |

## 5.1 Transient thermal impedance

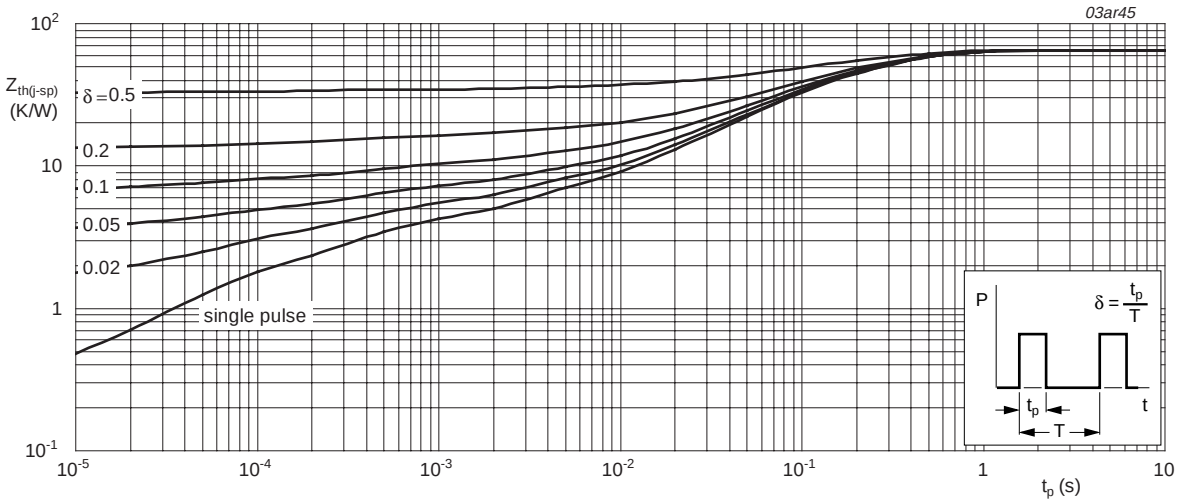


**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.**


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## 6. Characteristics

**Table 5: Characteristics**

*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = –250 µA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | –20 | - | - | V |
| | | $T_j$ = –55 °C | –18 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = –1 mA; $V_{DS}$ = $V_{GS}$; Figure 9 and 10 | | | | |
| | | $T_j$ = 25 °C | –0.55 | –0.75 | –0.95 | V |
| | | $T_j$ = 150 °C | –0.35 | - | - | V |
| | | $T_j$ = –55 °C | - | - | –1.1 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = –20 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | –1 | µA |
| | | $T_j$ = 150 °C | - | - | –100 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±12 V; $V_{DS}$ = 0 V | - | –10 | –100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = –4.5 V; $I_D$ = –2.8 A; Figure 6 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 65 | 76 | mΩ |
| | | $T_j$ = 150 °C | - | 104 | 122 | mΩ |
| | | $V_{GS}$ = –2.5 V; $I_D$ = –2.3 A; Figure 6 and 8 | - | 90 | 112 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = –2.8 A; $V_{DS}$ = –6 V; $V_{GS}$ = –4.5 V; Figure 11 | - | 7.6 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 1.6 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 0.65 | - | nC |
| $V_{plat}$ | plateau voltage | | - | –1.5 | - | V |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = –20 V; f = 1 MHz; Figure 13 | - | 725 | - | pF |
| $C_{oss}$ | output capacitance | | - | 105 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 80 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = –6 V; $R_L$ = 6 Ω; $V_{GS}$ = –4.5 V; $R_G$ = 6 Ω | - | 7 | - | ns |
| $t_r$ | rise time | | - | 21 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 68 | - | ns |
| $t_f$ | fall time | | - | 33 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = –1.25 A; $V_{GS}$ = 0 V; Figure 12 | - | –0.77 | –1.2 | V |



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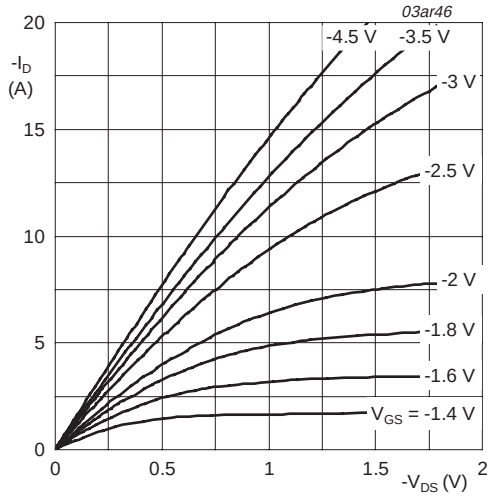
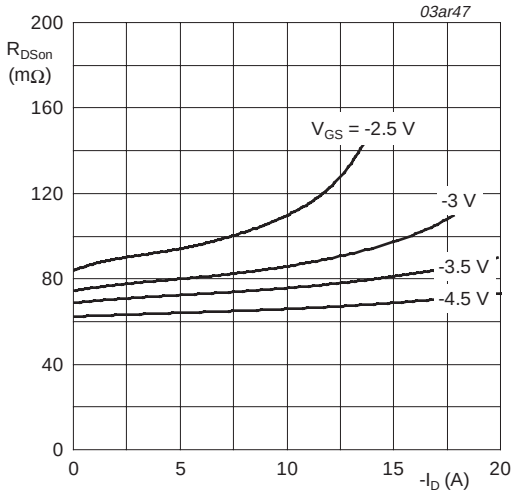


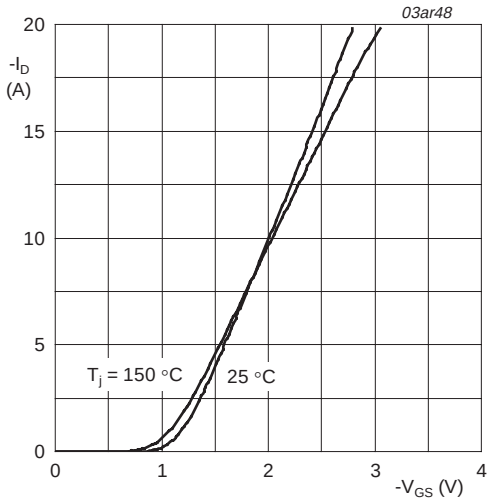

$T_j$ = 25 °C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



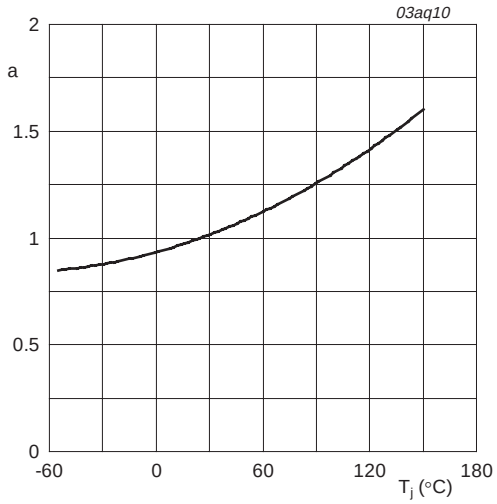

$T_j$ = 25 °C

**Fig 6. Drain-source on-state resistance as a function of drain current; typical values.**




$T_j$ = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**




$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**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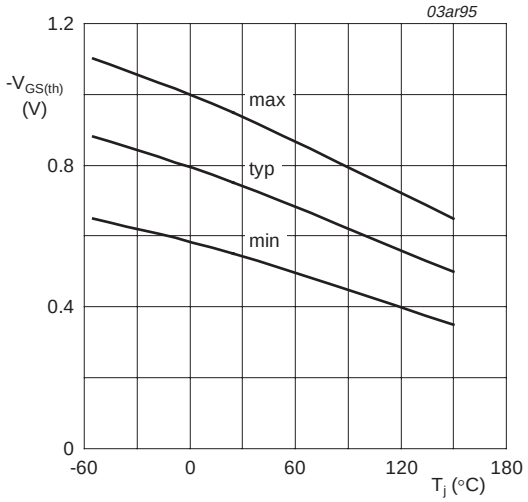
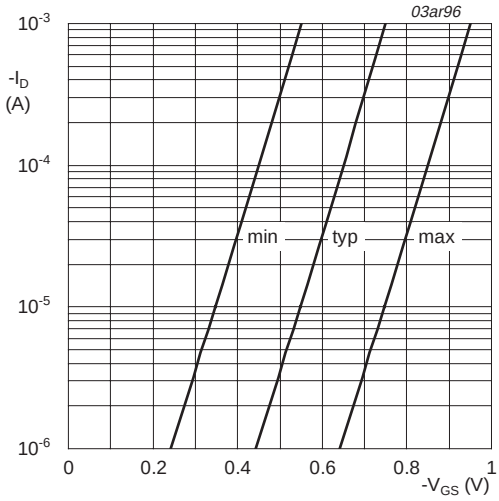


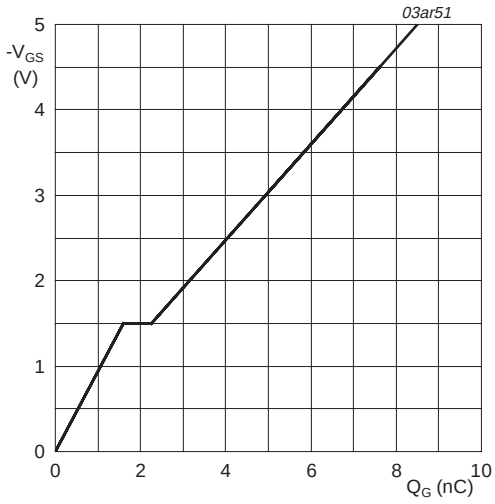

$I_D$ = –1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**




$T_j$ = 25 °C; $V_{DS}$ = –5 V

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**




$I_D$ = –2.8 A; $V_{DS}$ = –6 V

**Fig 11. Gate-source voltage as a function of gate charge; typical values.**



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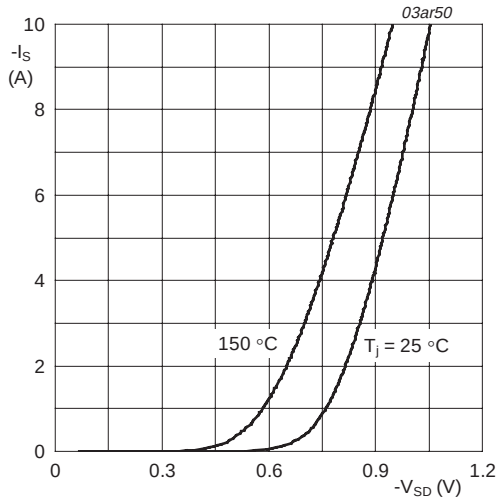
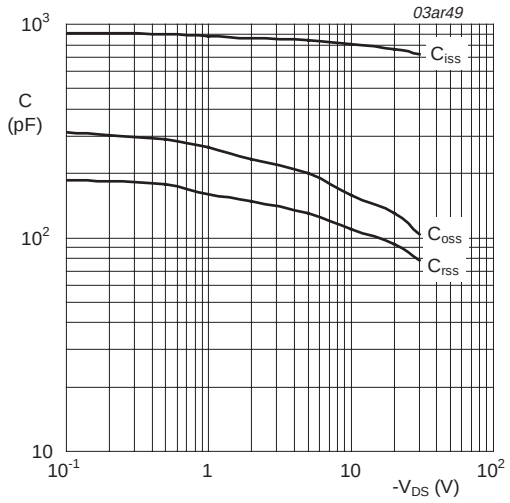



$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**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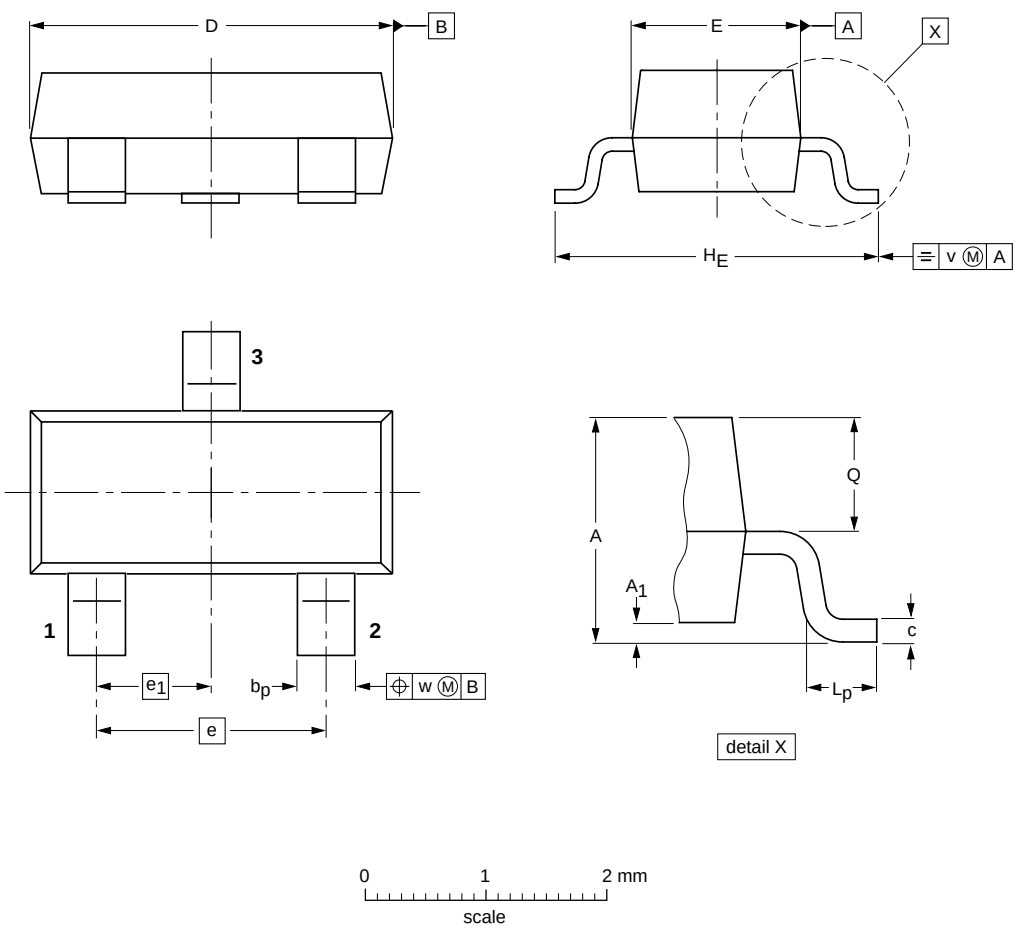
## 7. Package outline

**Plastic surface mounted package; 3 leads** **SOT23**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ max. | $b_p$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.1 | 0.48<br>0.38 | 0.15<br>0.09 | 3.0<br>2.8 | 1.4<br>1.2 | 1.9 | 0.95 | 2.5<br>2.1 | 0.45<br>0.15 | 0.55<br>0.45 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT23 | | TO-236AB | | | | ~~97-02-28~~<br>99-09-13 |

**Fig 14. SOT23 package outline.**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## 8. Revision history

**Table 6: Revision history**

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|---|---|---|---|---|---|
| PMV65XP_1 | 20040928 | Product data sheet | - | 9397 750 13993 | - |


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|---|---|---|---|
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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