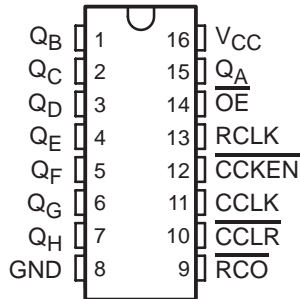


SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

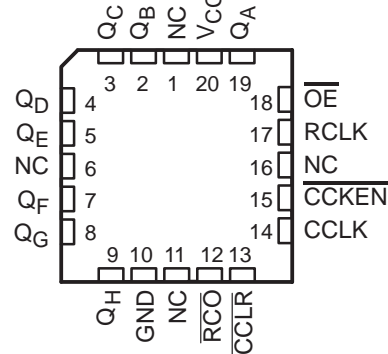
SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

- 2-V to 6-V V_{CC} Operation
- High-Current 3-State Parallel Register Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- 8-Bit Counter With Register
- Counter Has Direct Clear

SN54HC590A . . . J OR W PACKAGE
SN74HC590A . . . D, DW, OR N PACKAGE
(TOP VIEW)



SN54HC590A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC590A devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear (\overline{CCLR}) and count-enable (\overline{CCKEN}) inputs. A ripple-carry output (\overline{RCO}) is provided for cascading. Expansion is accomplished easily for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to the counter clock (CCLK) input of the following stage.

CCLK and the register clock (RCLK) inputs are positive-edge triggered. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC590AN | SN74HC590AN |
| | SOIC – D | Tube of 40 | SN74HC590AD | HC590A |
| | | Reel of 2500 | SN74HC590ADR | |
| | | Reel of 250 | SN74HC590ADT | |
| | SOIC – DW | Tube of 40 | SN74HC590ADW | HC590A |
| Reel of 2000 | | SN74HC590ADWR | | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC590AJ | SNJ54HC590AJ |
| | CFP – W | Tube of 150 | SNJ54HC590AW | SNJ54HC590AW |
| | LCCC - FK | Tube of 55 | SNJ54HC590AFK | SNJ54HC590AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

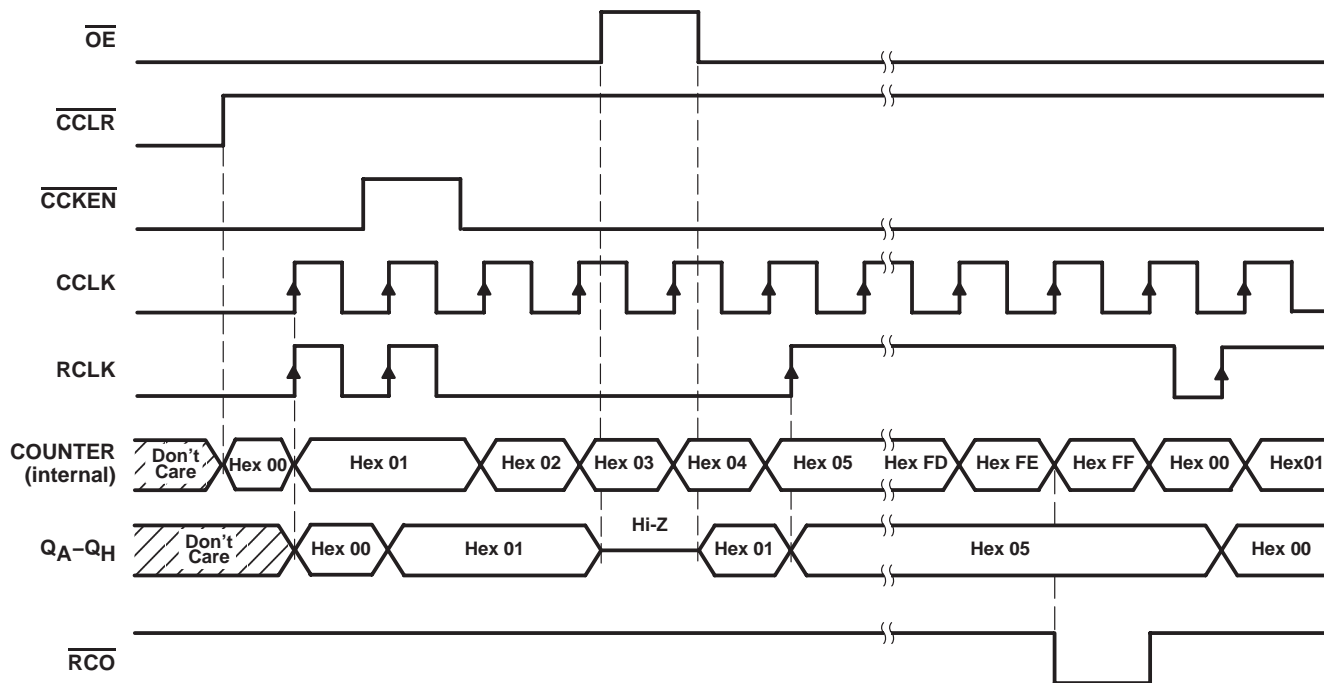
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

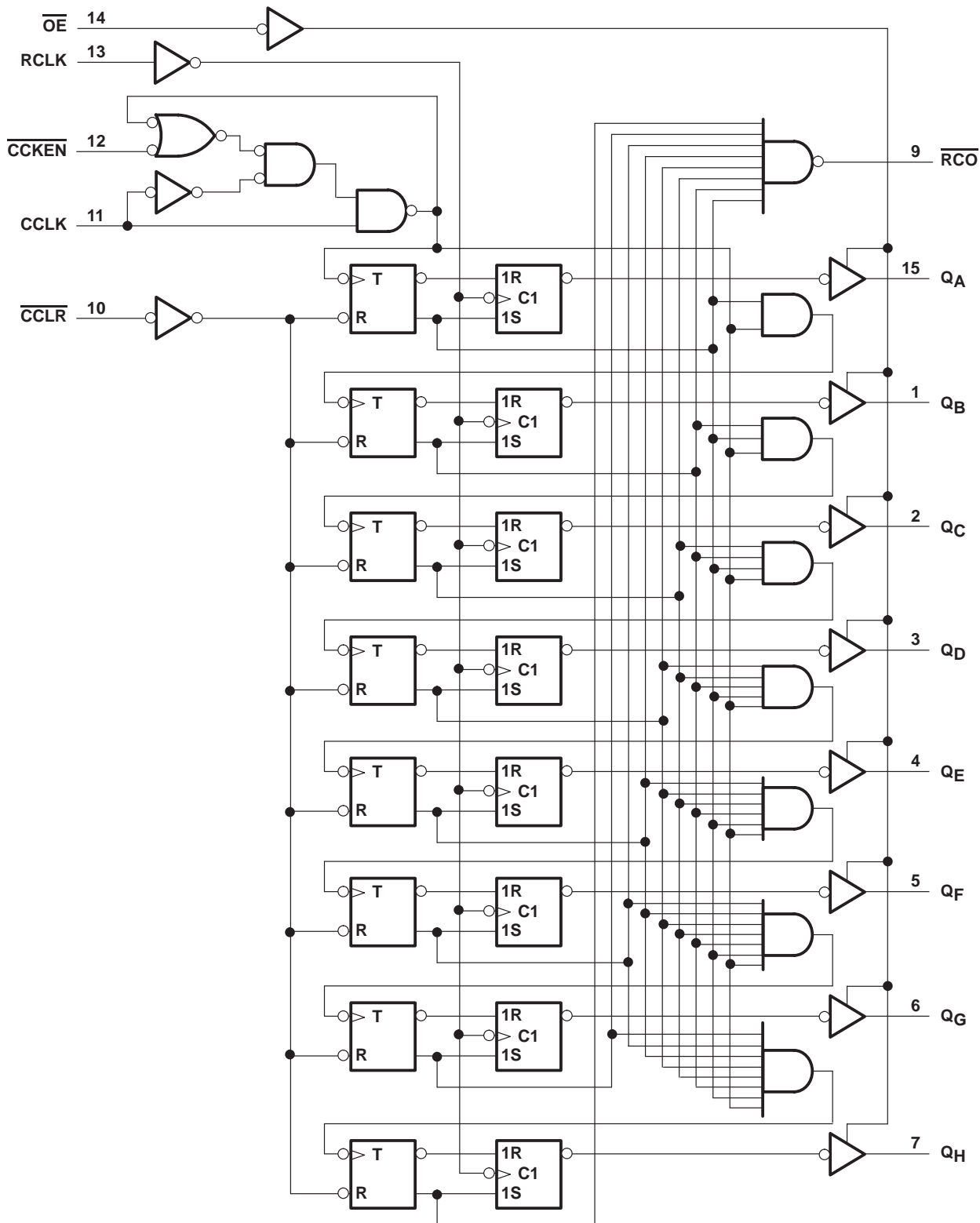
timing diagram



TIMING SEQUENCE

1. Clear Counter (asynchronous).
2. Count up: 0x01. Store 0x00 in register.
3. Inhibit counter clock (CCKEN = HIGH). Store 0x01 in register.
4. Count 0x02, 0x03.
5. 3-state the outputs
6. Count up: 0x04
7. Enable outputs.
8. Continue up: 0x05
9. Store 0x05 in register.
10. Continue counting: 0x06...0xFD, 0xFE, 0xFF, 0x00, etc.
11. Store 0x00 in register.

logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.

SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 35 mA |
| Continuous current through V_{CC} or GND | ± 70 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| DW package | 57°C/W |
| N package | 67°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | SN54HC590A | | | SN74HC590A | | | UNIT |
|----------------|---------------------------------------|------------------|----------|------|------------|----------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | | 1.5 | 1.5 | | V | |
| | | $V_{CC} = 4.5$ V | | 3.15 | 3.15 | | | |
| | | $V_{CC} = 6$ V | | 4.2 | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.5 | 0.5 | | V | |
| | | $V_{CC} = 4.5$ V | | 1.35 | 1.35 | | | |
| | | $V_{CC} = 6$ V | | 1.8 | 1.8 | | | |
| V_I | Input voltage | 0 | V_{CC} | | 0 | V_{CC} | | V |
| V_O | Output voltage | 0 | V_{CC} | | 0 | V_{CC} | | V |
| t_t^\ddagger | Input transition (rise and fall) time | $V_{CC} = 2$ V | | 1000 | 1000 | | ns | |
| | | $V_{CC} = 4.5$ V | | 500 | 500 | | | |
| | | $V_{CC} = 6$ V | | 400 | 400 | | | |
| T_A | Operating free-air temperature | -55 | 125 | | -40 | 85 | | °C |

‡ If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CCLK and RCLK inputs are not ensured while in the shift, count, or toggle operating modes.

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
 SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54HC590A | | SN74HC590A | | UNIT |
|-----------------|--|--------------------------|--|-------|-------|------------|-------|------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | |
| | | 4.5 V | \overline{RCO} , I _{OH} = -4 mA | 3.98 | 4.3 | | 3.7 | | 3.84 | |
| | | | Q _A -Q _H , I _{OH} = -6 mA | 3.98 | 4.3 | | 3.7 | | 3.84 | |
| | | | \overline{RCO} , I _{OH} = -5.2 mA | 5.48 | 5.8 | | 5.2 | | 5.34 | |
| 6 V | Q _A -Q _H , I _{OH} = -7.8 mA | 5.48 | 5.8 | | 5.2 | | 5.34 | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | 0.1 | |
| | | 4.5 V | \overline{RCO} , I _{OL} = 4 mA | | 0.17 | 0.26 | | 0.4 | 0.33 | |
| | | | Q _A -Q _H , I _{OL} = 6 mA | | 0.17 | 0.26 | | 0.4 | 0.33 | |
| | | | \overline{RCO} , I _{OL} = 5.2 mA | | 0.15 | 0.26 | | 0.4 | 0.33 | |
| 6 V | Q _A -Q _H , I _{OL} = 7.8 mA | | 0.15 | 0.26 | | 0.4 | 0.33 | | | |
| I _I | V _I = V _{CC} or 0 | 6 V | | ±0.1 | ±100 | | ±1000 | ±1000 | nA | |
| I _{OZ} | V _O = V _{CC} or 0 | 6 V | | ±0.01 | ±0.5 | | ±10 | ±5 | μA | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 6 V | | | 8 | | 160 | 80 | μA | |
| C _i | | 2 V to 6 V | | 3 | 10 | | 10 | 10 | pF | |

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC590A | | SN74HC590A | | UNIT |
|--------------------|-----------------------------------|-----------------|-----------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | 4 | | 2.5 | | 3.2 | | MHz |
| | | 4.5 V | 20 | | 13 | | 16 | | |
| | | 6 V | 24 | | 16 | | 19 | | |
| t _w | CCLK or RCLK high or low | 2 V | 125 | | 200 | | 155 | | ns |
| | | 4.5 V | 25 | | 38 | | 31 | | |
| | | 6 V | 21 | | 32 | | 26 | | |
| | CCLR low | 2 V | 100 | | 150 | | 125 | | |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 26 | | 21 | | |
| t _{su} | CCKEN low before CCLK↑ | 2 V | 100 | | 150 | | 125 | | ns |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 26 | | 21 | | |
| | CCLR high (inactive) before CCLK↑ | 2 V | 100 | | 150 | | 125 | | |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 26 | | 21 | | |
| | CCLK↑ before RCLK↑† | 2 V | 100 | | 150 | | 125 | | |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 26 | | 21 | | |
| t _h | CCKEN low after CCLK↑ | 2 V | 50 | | 75 | | 60 | | ns |
| | | 4.5 V | 10 | | 15 | | 12 | | |
| | | 6 V | 9 | | 13 | | 11 | | |

† This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.



SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | SN54HC590A | | | | UNIT | |
|------------------|------------------------------------|-------------------------|----------|--------------------------|-----|-----|-----|------|-----|
| | | | | $T_A = 25^\circ\text{C}$ | | | MIN | | MAX |
| | | | | MIN | TYP | MAX | | | |
| f_{max} | | | 2 V | 4 | 8 | 2.5 | MHz | | |
| | | | 4.5 V | 20 | 35 | 13 | | | |
| | | | 6 V | 24 | 40 | 16 | | | |
| t_{pd} | CCLK \uparrow | $\overline{\text{RCO}}$ | 2 V | 80 | 150 | 225 | ns | | |
| | | | 4.5 V | 20 | 31 | 45 | | | |
| | | | 6 V | 15 | 26 | 38 | | | |
| t_{PLH} | $\overline{\text{CCLR}}\downarrow$ | $\overline{\text{RCO}}$ | 2 V | 70 | 130 | 195 | ns | | |
| | | | 4.5 V | 18 | 28 | 39 | | | |
| | | | 6 V | 14 | 23 | 33 | | | |
| t_{pd} | RCLK \uparrow | Q | 2 V | 70 | 140 | 210 | ns | | |
| | | | 4.5 V | 18 | 31 | 42 | | | |
| | | | 6 V | 14 | 25 | 36 | | | |
| t_{en} | $\overline{\text{OE}}\downarrow$ | Q | 2 V | 80 | 125 | 185 | ns | | |
| | | | 4.5 V | 20 | 30 | 37 | | | |
| | | | 6 V | 15 | 28 | 31 | | | |
| t_{dis} | $\overline{\text{OE}}\uparrow$ | Q | 2 V | 80 | 125 | 185 | ns | | |
| | | | 4.5 V | 20 | 30 | 37 | | | |
| | | | 6 V | 15 | 28 | 31 | | | |
| t_t^* | | $\overline{\text{RCO}}$ | 2 V | 38 | 75 | 110 | ns | | |
| | | | 4.5 V | 8 | 15 | 22 | | | |
| | | | 6 V | 6 | 13 | 19 | | | |
| | | Q | 2 V | 38 | 60 | 90 | | | |
| | | | 4.5 V | 8 | 12 | 18 | | | |
| | | | 6 V | 6 | 10 | 15 | | | |

* This parameter is not production tested for the SN54HC590A.

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | SN74HC590A | | | | UNIT | |
|------------------|---------------------|------------------|-----------------|-----------------------|-----|-----|-----|------|-----|
| | | | | T _A = 25°C | | | MIN | | MAX |
| | | | | MIN | TYP | MAX | | | |
| f _{max} | | | 2 V | 4 | 8 | 3.2 | MHz | | |
| | | | 4.5 V | 20 | 35 | 16 | | | |
| | | | 6 V | 24 | 40 | 19 | | | |
| t _{pd} | CCLK↑ | \overline{RCO} | 2 V | | 80 | 150 | 190 | ns | |
| | | | 4.5 V | | 20 | 30 | 38 | | |
| | | | 6 V | | 15 | 26 | 33 | | |
| t _{PLH} | \overline{CCLR} ↓ | \overline{RCO} | 2 V | | 70 | 130 | 165 | ns | |
| | | | 4.5 V | | 18 | 26 | 33 | | |
| | | | 6 V | | 14 | 22 | 28 | | |
| t _{pd} | RCLK↑ | Q | 2 V | | 70 | 140 | 175 | ns | |
| | | | 4.5 V | | 18 | 28 | 35 | | |
| | | | 6 V | | 14 | 24 | 30 | | |
| t _{en} | \overline{OE} ↓ | Q | 2 V | | 80 | 125 | 155 | ns | |
| | | | 4.5 V | | 20 | 25 | 31 | | |
| | | | 6 V | | 15 | 21 | 26 | | |
| t _{dis} | \overline{OE} ↑ | Q | 2 V | | 80 | 125 | 155 | ns | |
| | | | 4.5 V | | 20 | 25 | 31 | | |
| | | | 6 V | | 15 | 21 | 26 | | |
| t _t | | \overline{RCO} | 2 V | | 38 | 75 | 95 | ns | |
| | | | 4.5 V | | 8 | 15 | 19 | | |
| | | | 6 V | | 6 | 13 | 16 | | |
| | | Q | 2 V | | 38 | 60 | 75 | | |
| | | | 4.5 V | | 8 | 12 | 15 | | |
| | | | 6 V | | 6 | 10 | 13 | | |

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | SN54HC590A | | | | UNIT | |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----|------|-----|
| | | | | $T_A = 25^\circ\text{C}$ | | | MIN | | MAX |
| | | | | MIN | TYP | MAX | | | |
| t_{pd} | RCLK \uparrow | Q | 2 V | 100 | 300 | 447 | ns | | |
| | | | 4.5 V | 24 | 60 | 90 | | | |
| | | | 6 V | 20 | 51 | 77 | | | |
| t_{en} | \overline{OE} | Q | 2 V | 90 | 200 | 300 | ns | | |
| | | | 4.5 V | 23 | 40 | 60 | | | |
| | | | 6 V | 19 | 34 | 51 | | | |
| t_t^* | | Q | 2 V | 45 | 210 | 315 | ns | | |
| | | | 4.5 V | 17 | 42 | 63 | | | |
| | | | 6 V | 13 | 36 | 53 | | | |

* This parameter is not production tested for the SN54HC590A.

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

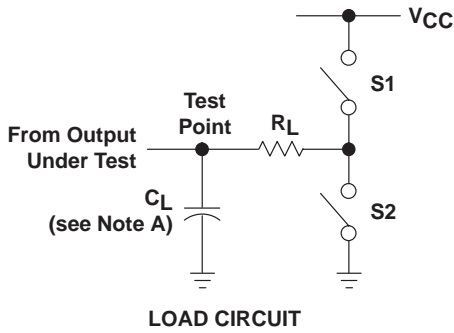
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | SN74HC590A | | | | UNIT | |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----|------|-----|
| | | | | $T_A = 25^\circ\text{C}$ | | | MIN | | MAX |
| | | | | MIN | TYP | MAX | | | |
| t_{pd} | RCLK \uparrow | Q | 2 V | 100 | 300 | 380 | ns | | |
| | | | 4.5 V | 24 | 60 | 76 | | | |
| | | | 6 V | 20 | 51 | 65 | | | |
| t_{en} | \overline{OE} | Q | 2 V | 90 | 200 | 250 | ns | | |
| | | | 4.5 V | 23 | 40 | 50 | | | |
| | | | 6 V | 19 | 34 | 43 | | | |
| t_t | | Q | 2 V | 45 | 210 | 265 | ns | | |
| | | | 4.5 V | 17 | 42 | 53 | | | |
| | | | 6 V | 13 | 36 | 45 | | | |

operating characteristics, $T_A = 25^\circ\text{C}$

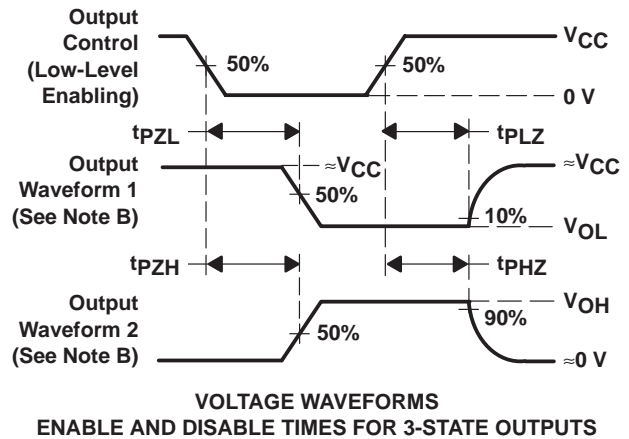
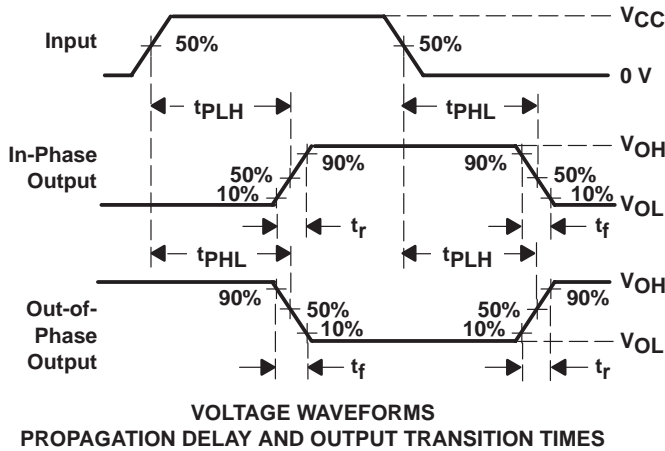
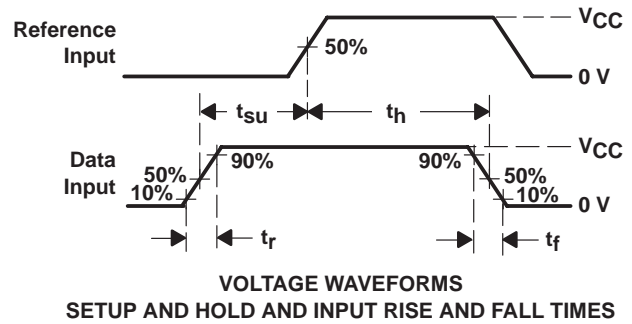
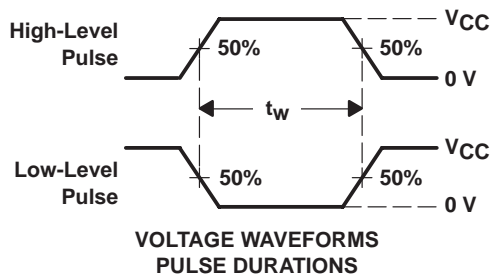
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance | No load | 250 | pF |

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
 SCLS039F – DECEMBER 1982 – REVISED SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | -- | 50 pF or 150 pF | Open | Open |



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{pZL} and t_{pZH} are the same as t_{dis} .
 F. t_{pZL} and t_{pZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| 5962-89603012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-89603012A SNJ54HC 590AFK | Samples |
| 5962-8960301EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8960301EA SNJ54HC590AJ | Samples |
| 5962-8960301FA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8960301FA SNJ54HC590AW | Samples |
| SN54HC590AJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HC590AJ | Samples |
| SN74HC590AD | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC590A | Samples |
| SN74HC590ADE4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC590A | Samples |
| SN74HC590ADG4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC590A | Samples |
| SN74HC590ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC590A | Samples |
| SN74HC590ADT | ACTIVE | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC590A | Samples |
| SN74HC590ADW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC590A | Samples |
| SN74HC590ADWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC590A | Samples |
| SN74HC590AN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC590AN | Samples |
| SN74HC590ANE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC590AN | Samples |
| SNJ54HC590AFK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-89603012A SNJ54HC 590AFK | Samples |
| SNJ54HC590AJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8960301EA SNJ54HC590AJ | Samples |
| SNJ54HC590AW | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8960301FA SNJ54HC590AW | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC590A, SN74HC590A :

● Catalog : [SN74HC590A](#)

● Military : [SN54HC590A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC590ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC590ADWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC590ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HC590ADWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-89603012A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 5962-8960301FA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74HC590AD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74HC590ADE4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74HC590ADG4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74HC590ADW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74HC590AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC590AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC590ANE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC590ANE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC590AFK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC590AW | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A



DW0016A

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

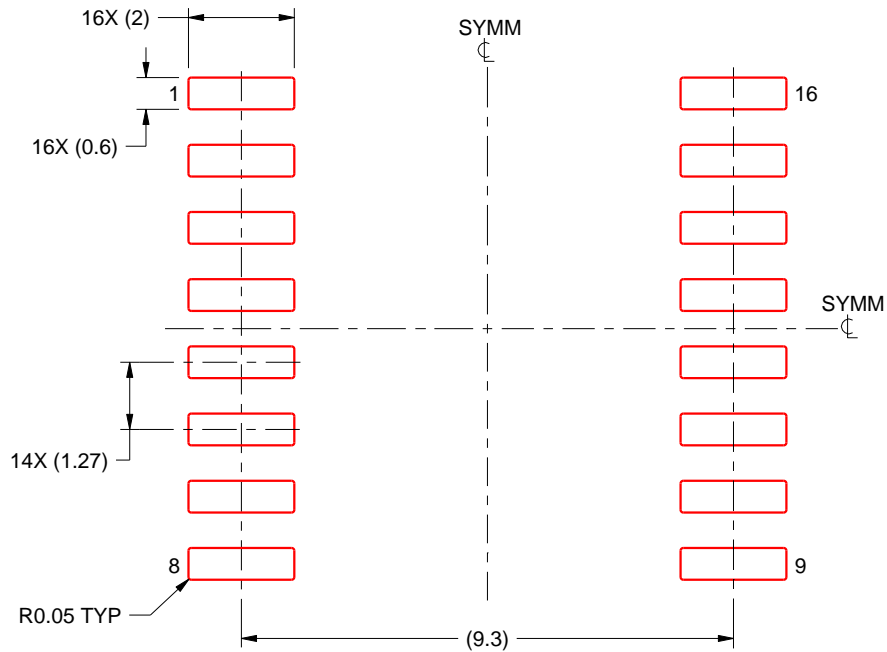
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated