Intel® Edison Module

Hardware Guide

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Revision History

Revision	Description	Date
ww32	Initial release	August 4, 2014
ww34	Minor edits.	August 20, 2014
001	First public release.	September 9, 2014
002	Minor corrections.	September 16, 2014

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1 Introduction

This document describes the hardware interface of the Intel® Edison compute module. It provides an overview of how to create an expansion board that connects directly to Edison.

1.1 References

Table 1 Product-specific documents

Reference	Name	Number/location
331188	Intel® Edison Board Support Package User Guide	
331189	Intel® Edison Module Hardware Guide	(This document)
331190	Intel® Edison Breakout Board Hardware Guide	
331191	Intel® Edison Kit for Arduino* Hardware Guide	
331192	Intel® Edison Native Application Guide	
331193	Intel® Edison Quick Start Guide	
[RN]	Intel® Edison Board Support Package Release Notes	
[GSG]	Intel® Edison Getting Started Guide	

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2 High-Level Functional Description

The Intel® Edison compute module is designed to lower the barriers to entry for anyone prototyping and producing IoT and wearable computing products. Intel® Edison contains the core system processing and connectivity elements: processor, PMIC, RAM, eMMC, and Wi-Fi/BT. It is not a self-contained, standalone device. Intel® Edison is a module that interfaces with end-user systems via a 70-pin connector. The Intel® Edison compute module does not include any video input or output interfaces (MIPI CSI, MIPI DSI, HDMI, etc.). Internal image processing and graphics processing cores are disabled (ISP, PowerVR, VED, VEC, VSP, etc.). Intel® Edison relies on the end-user support of input power. (in other words, the Intel® Edison compute module does not necessarily control battery recharging). Table 2 shows the main system components.

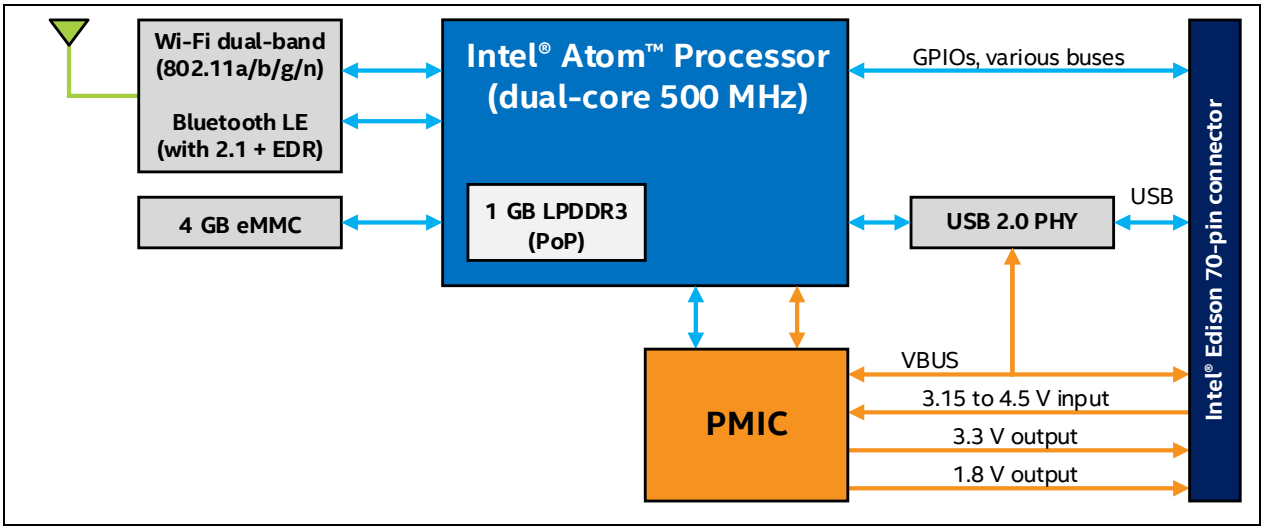
Table 2 Hardware features

Component	Description
Processor	Dual Core IA-32 @ 500 MHz, 32-bit Intel® Atom™ Processor Z34xx Series @ 100 MHz
RAM	1 GB LPDDR3 POP memory (2 channel 32 bits @ 800 MT/sec)
Internal storage	4 GB eMMC (v4.51 spec)
Power	TI SNB9024 power management IC
Wireless	Dual-band (2.4 and 5 GHz) IEEE 802.11a/b/g/n
Bluetooth*	BT 4.0 + 2.1 EDR
Antenna	Dual-band onboard chip antenna or u.FL for external antenna
Connector	70-pin Hirose DF40 Series (1.5, 2.0, or 3.0 mm stack height)
Size	35.5 × 25.0 × 3.9 mm maximum (to be verified)
Power input	3.15 to 4.5 V
I/O	40 general purpose GPIO which can be configured as: • SD card: 1 interface • UART: 2 controllers (one full flow control, one Rx/Tx) • I^2C: 2 controllers • SPI: 1 controller with 2 chip selects • I2S: 1 controller • GPIO: Additional 14 (with 4 capable of PWM)
USB 2.0	1 OTG controller
Clocks	19.2 MHz, 32 kHz

2.1 Block diagram

Figure 1 shows the basic Edison block diagram.

Figure 1 Edison block diagram



2.2 Module photos

Figure 2 Edison top view

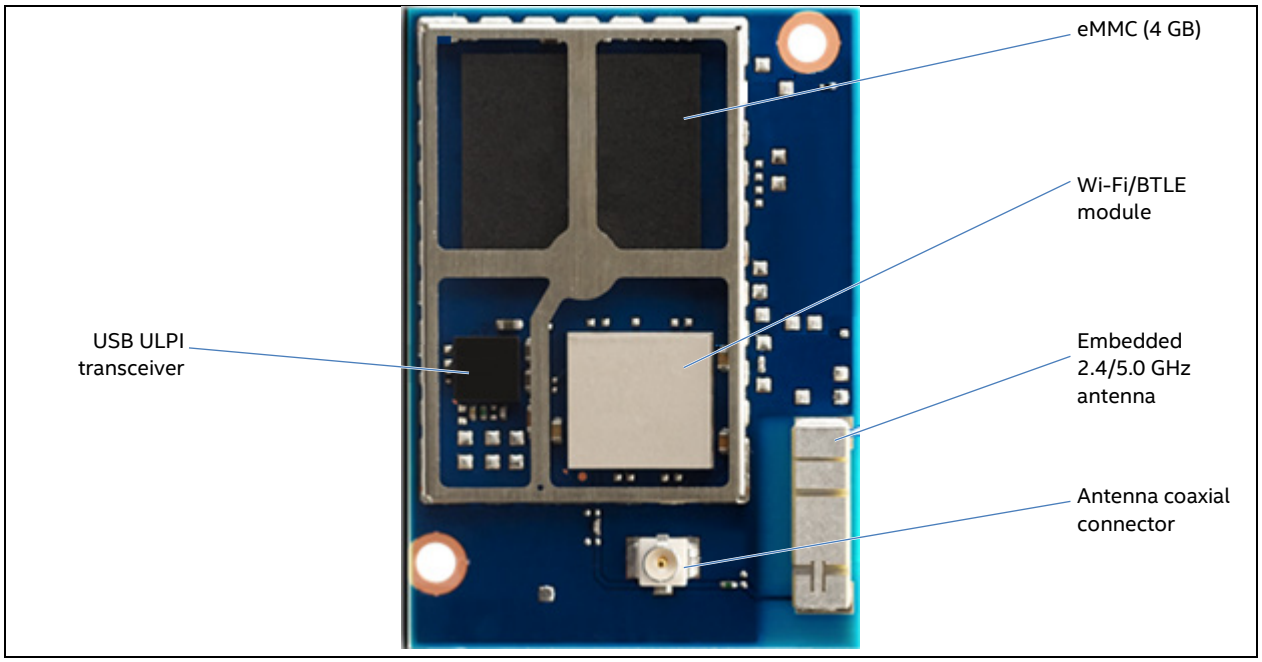
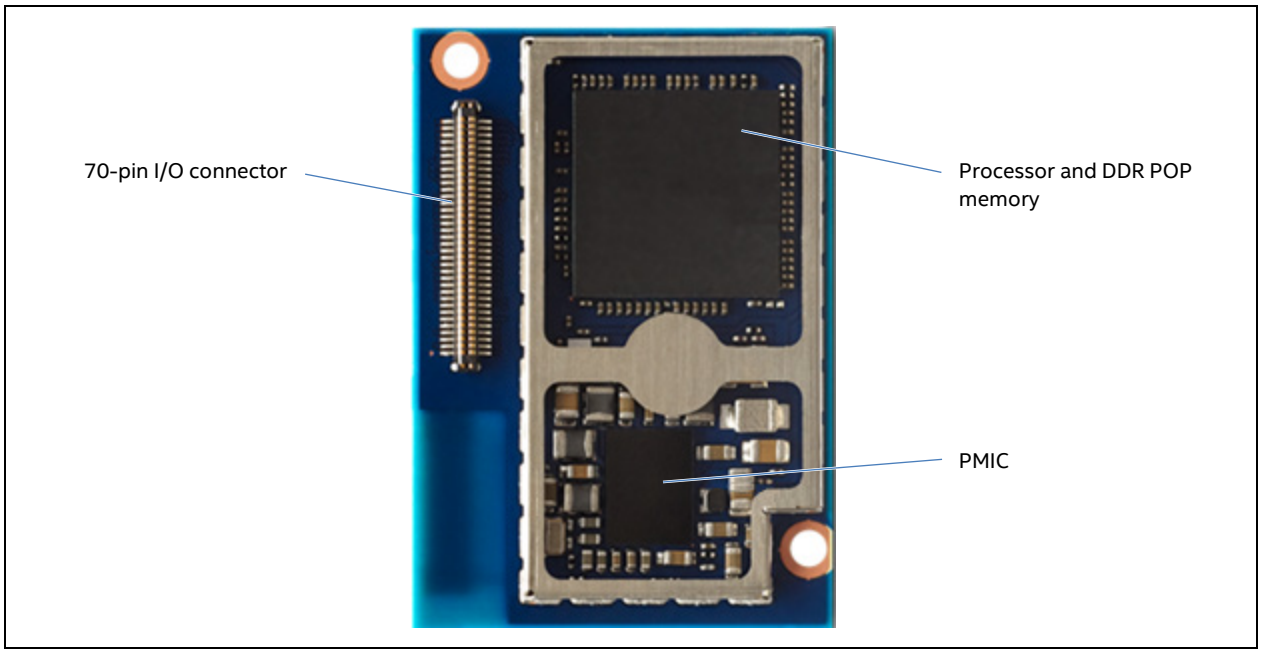


Figure 3 Edison bottom view



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3 Component and Subsystem Details

3.1 Intel® Atom™ processor Z34XX

Intel® Atom™ Processor Z34xx Series is the next generation 22 nm SoC product targeted for the smartphone market segment. The SoC contains dual IA-32 cores operating at 500 MHz. The architecture includes 2-wide instruction decode and Out Of Order Execution with 1 MB cache shared between the two CPU cores. It includes Intel SIMD Extensions 2, 3, 4 (SSE2, SSE3, SSE4.1/4.2).

3.2 Wi-Fi / BT module

The Murata integrated Wi-Fi BT module is built around a Broadcom BCM43340 Wi-Fi /BT device.

The Broadcom BCM43340 single chip quad device provides the highest level of integration for a mobile or handheld wireless system, with integrated dual band (2.4 / 5 GHz) IEEE 802.11a/b/g/n MAC/baseband/radio with Bluetooth 4.0.

- Dual-band 2.4 GHz and 5 GHz IEEE 802.11 a/b/g/n.
- Single-stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 150 Mbps for typical upper layer throughput in excess of 90 Mbps.
- Supports standard SDIO v2.0 and gSPI (48 MHz) host interfaces.
- Complies with Bluetooth* Core Specification Version 4.0 with provisions for supporting future specifications. Bluetooth Class 1 or Class 2 transmitter operation.
- Security:
  - WPA and WPA2 (personal) support for powerful encryption and authentication.
  - AES in WLAN hardware for faster data encryption and IEEE 802.11i compatibility –Reference WLAN subsystem provides Cisco* Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0).
  - Reference WLAN subsystem provides Wi-Fi protected setup (WPS).

3.3 Managed NAND (eMMC) flash

Edison uses 4 GB of managed NAND to store the file system and user data. Managed NAND flash contains a full MMC controller, wear-leveling firmware, and all the other features that are typically found in MMC cards, except it is available in a small BGA form-factor.

- Bus mode
  - Data bus width: 1 bit (default), 4 bits, 8 bits
  - Data transfer rate: up to 200 MBps (HS200)
  - MMC I/F clock frequency: 0~200 MHz
  - MMC I/F boot frequency: 0~52 MHz

3.4 DDR SDRAM

Edison supports 1 GB LPDDR3 memory at speeds up to 1033 MT/s.

- 8 banks
- Row addresses R0-R13
- Column addresses C0-C9
- Dual-channel 32 bits
- 400 MHz clock max (800 MT/s)

3.5 Power management IC (PMIC)

Edison uses the Texas Instruments* SNB9024 Power Management Integrated Circuit (PMIC). The SNB9024 PMIC is for mobile application processors platforms with high feature integration in order to minimize system board area. It includes subsystems for voltage regulation, A/D conversion, GPIOs, and RTC. The SNB9024 device is controlled and programmed using an I^2C interface. There is also a serial voltage ID interface between the SOC and PMIC for handling core voltage rail settings as well as system control signals.

- Four high-efficiency buck converters
  - – Two dual-phase 0.55 to 1.2 V @ 4.8 A with DVS
  - – One dual-phase 1.24 V @ 2.5 A
  - – One single-phase 1.8 V @ 1.1 A
- One 5 V 1.2 A boost converter
- One 3.3 V/3.4 V 1.4 A buck-boost converter
- Five low drop-out regulators
  - – Three programmable 1.05 to 2.85 V @ 100 to 300 mA
  - – One high precision 1 V @ 2 mA
  - – One DVS 0.75 to 0.95 V @ 220 mA
- Two load switches with slew rate control and external load switch control
- USB and AC/DC adapter power supply detection with external charger control (enable/disable and current limit)
- I^2C Interface and dedicated SVI
- Interrupt controller for PMIC events
- Seven general purpose 1.8 V I/Os, with two of them supporting up to 3.3 V
- 32.768 kHz RTC for backup time
- Alarm timer interrupt
- Sleep clock outputs (32.768 kHz)

3.6 USB 2.0 transceiver ULPI interface

The TUSB1211 is a USB 2.0 transceiver chip, designed to interface with a USB controller via a ULPI interface. It supports all USB 2.0 data rates (High-Speed 480 Mbps, Full-Speed 12 Mbps and Low-Speed 1.5 Mbps) in both Host and Peripheral modes. TUSB1211 also supports the OTG (Ver1.3) optional addendum to the USB 2.0 specification, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).

TUSB1211 also supports USB Battery Charging Specification v1.1 integrating a charger detection module for sensing and control on DP/DM lines, and ACA (Adaptive Charger Accessory) detection and control on ID line. ACA allows simultaneous connection of a USB Charger or Charging Downstream Port and an Accessory to a portable OTG device. Configuration bits allow an ACA-agnostic legacy link to correctly communicate with the connected accessory port through the ACA.

3.7 Integrated chip antenna or u.FL connector for external antenna

The Edison module has an integrated dual-band 2.4/5 GHz antenna built onboard. The onboard antenna is used primarily for small form factor plastic devices. For larger devices or a device which has a metal enclosure, another version of Edison is available with an industry standard u.FL connector for attachment to an external antenna. This will allow the end-user to locate the antenna for optimal performance.

3.8 70-pin interface connector

The Edison module connects to the end user device via a 70-pin connector. The connector on Edison is a Hirose 70-pin DF40 Series “header” connector sometimes referred to as a “plug” connector. The Hirose part number for the “header” connector on Edison is: DF40C-70DP-0.4V(51).

The mating Hirose connector on an expansion board is the “receptacle” connector. This mating “receptacle” connector is available in three different heights. The board-to-board mating stack height can be 1.5, 2.0, or 3.0 mm. Table 3 lists the Hirose part number for the “receptacle” connector and corresponding DigiKey and Mouser part numbers for an expansion board.

Table 3 Edison 70-pin connector part numbers

Hirose P/N	Mating stack height	DigiKey P/N	Mouser P/N
DF40C-70DS-0.4V(51)	1.5 mm	n/a	798-DF40C70DS04V51
DF40C(2.0)-70DS-0.4V(51)	2.0 mm	H11908CT-ND (low quantity) H11908TR-ND (tape and reel)	798-DF40C2070DS04V51
DF40HC(3.0)-70DS-0.4V(51)	3.0 mm	n/a	n/a

The Edison Arduino board utilizes the 2.0 mm board-to-board stack height connector.

The bottom side of Edison (side with 70-pin connector) has a component height (shield height) of 1.5 mm and will sit flush against the connecting PCB if a 1.5 mm connector is used. Table 3 lists the expansion board component height restrictions for components under Edison.

Table 4 Edison 70-pin connector board-to-board mating height

Hirose P/N	Board-to-board mating height	Available height under Edison
DF40C-70DS-0.4V(51)	1.5 mm	n/a
DF40C(2.0)-70DS-0.4V(51)	2.0 mm	0.5 mm
DF40HC(3.0)-70DS-0.4V(51)	3.0 mm	1.5 mm

Edison is secured to an expansion board via two mounting holes each with a diameter of 2.0 mm. Any mounting standoffs will also need to match the mating connector height (1.5, 2.0, or 3.0 mm).

Table 5 lists the Edison 70-pin connector pinouts and signals.

Table 5 Edison connector pinout and signal list

Pin	Signal name	Alternate function	Description
2, 4, 6	VSYS		System input power (3.3 to 4.5 V)
8, 10	3.3 V		System 3.3 V output
12	1.8 V		System 1.8 V output (same as I/O voltage levels)
14	DCIN		Input, connect to VSYS when powering from a DC power adapter (no connect if powering from a battery)
1,5,9,11,13,15	GND		Ground
7	MSIC_SLP_CLK3		32 kHz sleep clock output
3	USB_ID		USB OTG ID pin
16	USB_DP		USB D+
18	USB_DN		USB D-
20	USB_VBUS		USB VBUS input (does not power system)
17	PWRBTN#		Power/sleep button input (active low)
19	FAULT		USB power fault input (from external USB current limit switch)
21	PSW		USB power output enable (to external USB current limit switch)
23	V_VBAT_BKUP		Real-time clock (RTC) backup battery input
36	RESET_OUT#		System reset output (active low)
24	GP44		GPIO
25	GP165		GPIO
26	GP45		GPIO
28	GP46		GPIO
30	GP47		GPIO
32	GP48		GPIO
34	GP49		GPIO
42	GP15		GPIO
48	GP14		GPIO
35	GP12_PWM0	PWM_0	GPIO, capable of PWM output
33	GP13_PWM1	PWM_1	GPIO, capable of PWM output
37	GP182_PWM2	PWM_2	GPIO, capable of PWM output
39	GP183_PWM3	PWM_3	GPIO, capable of PWM output
41	GP19	I2C_1_SCL	GPIO, I2C1 clock (open collector when configured for I^2C)
43	GP20	I2C_1_SDA	GPIO, I2C1 data (open collector when configured for I^2C)
45	GP27	I2C_6_SCL	GPIO, I2C6 clock (open collector when configured for I^2C)
47	GP28	I2C_6_SDA	GPIO, I2C6 data (open collector when configured for I^2C)
50	GP42	I2S_2_RXD	GPIO, I2S2 receive data (input)
52	GP40	I2S_2_CLK	GPIO, I2S2 clock (output)

Pin	Signal name	Alternate function	Description
54	GP41	I2S_2_FS	GPIO, I2S2 frame sync (output)
56	GP43	I2S_2_TXD	GPIO, I2S2 transmit data (output)
22	GP134	UART_2_RX	GPIO, UART2 receive (input)
27	GP135	UART_2_TX	GPIO, UART2 transmit (output)
51	GP111	SPI_2_FS1	GPIO, SPI2 chip select 1 (output)
53	GP110	SPI_2_FS0	GPIO, SPI2 chip select 0 (output)
55	GP109	SPI_2_CLK	GPIO, SPI2 clock output
57	GP115	SPI_2_TXD	GPIO, SPI2 transmit data (output)
59	GP114	SPI_2_RXD	GPIO, SPI2 receive data (input)
46	GP131	UART_1_TX	GPIO, UART1 transmit (output)
61	GP130	UART_1_RX	GPIO, UART1 receive data (input)
63	GP129	UART_1_RTS	GPIO, UART1 ready to send (output)
65	GP128	UART_1_CTS	GPIO, UART1 clear to send (input)
44	GP84	SD_0_CLK_FB	GPIO, SD clock feedback
58	GP78	SD_0_CLK	GPIO, SD clock output
60	GP77	SD_0_CD#	GPIO, SD card detect input (active low)
62	GP79	SD_0_CMD	GPIO, SD command
66	GP80	SD_0_DAT0	GPIO, SD data 0
70	GP81	SD_0_DAT1	GPIO, SD data 1
64	GP82	SD_0_DAT2	GPIO, SD data 2
68	GP83	SD_0_DAT3	GPIO, SD data
67	OSC_CLK_OUT_0		19.2 MHz high speed clock output
31	RCVR_MODE		Firmware recovery mode
69	FW_RCVR		Firmware recovery (active high on boot)
29,38,40,49	Unused.		

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4 External Interfaces on 70-Pin Connector

All Edison I/O (with the exception of USB) uses 1.8 V signaling.

4.1 I²C Interfaces

Edison has two available I²C interfaces, I2C1 and I2C6. I2C1 on pins 41 and 43 is a general purpose I²C interface that connects directly to the IA cores. I2C6 on pins 45 and 47 can be configured as I2C6 which connects to the IA cores or as I2C8 which connects to a system controller fabric (controlled by MCU). For the initial release of Edison, only I2C1 and I2C6 are available. Both of these interfaces are open collector when configured as I²C. When configured as GPIO, they can be standard push pull outputs.

The I²C module can operate in the following modes:

- Standard mode (with data rates up to 100 kbps).
- Fast mode (with data rates up to 400 kbps).
- High-speed mode (with data rates up to 3.4 Mbps).
- The SoC is always I²C master, it does not support multimaster mode.
- The SoC can support clock stretching by slave devices.
- Both 7-bit and 10-bit addressing modes are supported.

When I2C6 is configured as I2C8, it can only run in standard or fast mode.

4.2 SD card interface

An SD 3.0 compliant interface is available on pins 44, 58, 60, 62, 64, 66, 68, and 70.

SD memory key features

- Host clock up to 50 MHz
- Supports card detection (insertion/removal) with dedicated card detection signal only.
- Meets SD Host Controller Standard Specification version 3.0.
- Only supports SD memory
- Requires external level shifter for support of 2.85 V devices

4.3 UART interfaces

There are two UARTs available, UART1 with flow control and UART2 without flow control. The UART1 interface is available on pins 46, 63, 61, and 54. UART2 is on pins 22 and 27. The UARTs are:

- 16550 compliant
- 64-byte buffer size
- Baud rate from 300 bps to 3.686 Mbps.

The UART2 alternate function is as the Linux debug serial port.

4.4 SPI interface

An SPI interface is available on pins 51, 53, 55, 57, and 59. The interface has two available chip selects.

- In a single-frame transfer, the SoC supports all four possible combinations for the serial clock phase and polarity.
- In multiple frame transfer, the SoC supports SPH=1 and SPO= 0 or 1.
- The SoC may toggle the slave select signal between each data frame for SPH=0.
- 25 MHz Master mode, 16.67 MHz slave mode.

4.5 I2S interface

An I2S interface is available on pins 50, 52, 54, and 56. All of the I2S modes below have not been verified and are subject to change. Table 6 lists the available formats available on the I2S port.

Table 6 Edison I2S available formats

Mode	Priority	Frame rate	Bits/ sample	Number of slots	Frame-to-data offset	Frame polarity	Frame width	Frame rate inaccuracy	Notes
I2S master	1	192K, 96K, 48K, 16K, 8K	16, 24	2	1	0-left, 1-right	50/50	0%	Standard I2S protocol. 50% duty cycle on frame.
PCM slave - SFS	1	192K, 96K, 48K, 44.1K, 16K, 8K	16, 24	192 kHz: 2 96 kHz: 4 All else: 1 to 6	0	High			
PCM slave - LFS	1	192K, 96K, 48K, 44.1K, 16K, 8K	16, 24	192 kHz: 2 96 kHz: 4 All else: 1 to 6	0	High			
PCM master - SFS	1	192K, 96K, 48K, 16K, 8K	16, 24	192 kHz: 2 All else: 1 to 4	0	High	1 bit clockwide	0%	Rising edge frame sensitive. Design supports more frame-to-data offset options.
PCM master - LFS	1	192K, 96K, 48K, 16K, 8K	16, 24	192 kHz: 2 All else: 1 to 4	0	High	1-bit to *n*-bit clocks	0%	*n* is the width of one slot. Design supports width > 1 slot.
Left justified master	2	192K, 96K, 48K	16, 24	2	0	0-left, 1-right	50/50	0%	Design supports flipping polarity on the frame signal.
I2S slave	3	192K, 96K, 48K, 44.1K	16, 24	2	0	0-left, 1-right	50/50	0%	
Left justified slave	3	192K, 96K, 48K	16, 24	2	0	0-left, 1-right	50/50	0%	
Right justified	Not supported.								

4.6 PWM

There are four available GPIO that can be configured as PWM outputs. These are found on pins 33, 35, 37, and 39. The PWM resolution is 8 bits.

The main PWM variables that control PWM output are:

- The PWM output frequency and duty cycle can be estimated by the equations:
  - Target frequency ~= 19.2 MHz * Base_unit value/256
  - Target PWM duty cycle ~= PWM_on_time_divisor / 256

Table 7 shows some examples of PWM programming.

Table 7 Edison PWM programming examples

Integer part of PWM_base_unit (bits 29:22)	Fractional part of PWM_base_unit (bits 21:8)	Decimal base unit value	Base unit type	PWM frequency (Hz)	PWM period (µs)	Bits of resolution	PWM steps
0000_0000b	00_0100_0000_0000b	0.0625	fractional	4,688	213	8	0.39%
0000_0000b	00_0010_0000_0000b	0.03125	fract iona l	2,344	427	8	0.39%
0000_0000b	00_0001_0000_0000b	0.015625	fractional	1,172	853	8	0.39%
0000_0000b	00_0000_1000_0000b	0.0078125	fractional	586	1,707	8	0.39%
0000_0000b	00_0000_0100_0000b	0.00390625	fract iona l	293	3,413	8	0.39%
0000_0000b	00_0000_0010_0000b	0.00195325	fractional	146	6827	8	0.39%
0000_0000b	00_0000_0001_0000b	0.0009765625	fractional	73.2	13,653	8	0.39%
0000_0000b	00_0000_0000_1000b	0.00048828125	fract iona l	36.6	27,307	8	0.39%
0000_0000b	00_0000_0000_0100b	0.000244140625	fractiona l	18.3	54,613	8	0.39%
0000_0000b	00_0000_0000_0010b	0.0001220703125	fractional	9.2	109,227	8	0.39%
0000_0000b	00_0000_0000_0001b	0.00006103515625	fract iona l	4.6	218,453	8	0.39%
0000_0000b	00_0000_0010_0001b	0.00201416015625	fract iona l	151	6619	8	0.39%

4.7 GPIO

A number of general purpose I/Os are available on the external interface. These are found on pins: 24, 25, 26, 28, 30, 32, 34, 42, and 48. Some of these serve alternate functions of interrupts for external sensor support. All the interfaces listed in Section 4 (I2C, I2S, UART, etc.) if not used, can be turned into general purpose I/Os.

When the pin mode is chosen as GPIO, it can be programmed as an output or input. When programmed as an input, a GPIO can serve as an interrupt or wake source. Inputs have programmable pullups or pulldowns. Pullup value can be 2, 20, or 50 kohm. I^2C pins also have an additional 910 ohm value. When in general purpose mode, input GPIO signals enter a glitch filter by default, before reaching the edge detection registers.

To ensure that a pulse is detected by the edge detection register, the pulse should be five clock cycles long.

- 100 ns for a 50 MHz clock when SoC is in S0 state.
- 260 ns for 19.2 MHz clock when SoC is in S0i1 or S0i2 State.
- 155.5 µs for 32 kHz clock (RTC) when SoC is in S0i3 State.

Most GPIO-capable pins are configured as GPIO inputs during the assertion of all resets, and they remain inputs until configured otherwise. As outputs, the GPIOs can be individually cleared or set. They can be preprogrammed to either state when entering standby. Output drive is ±3 mA.

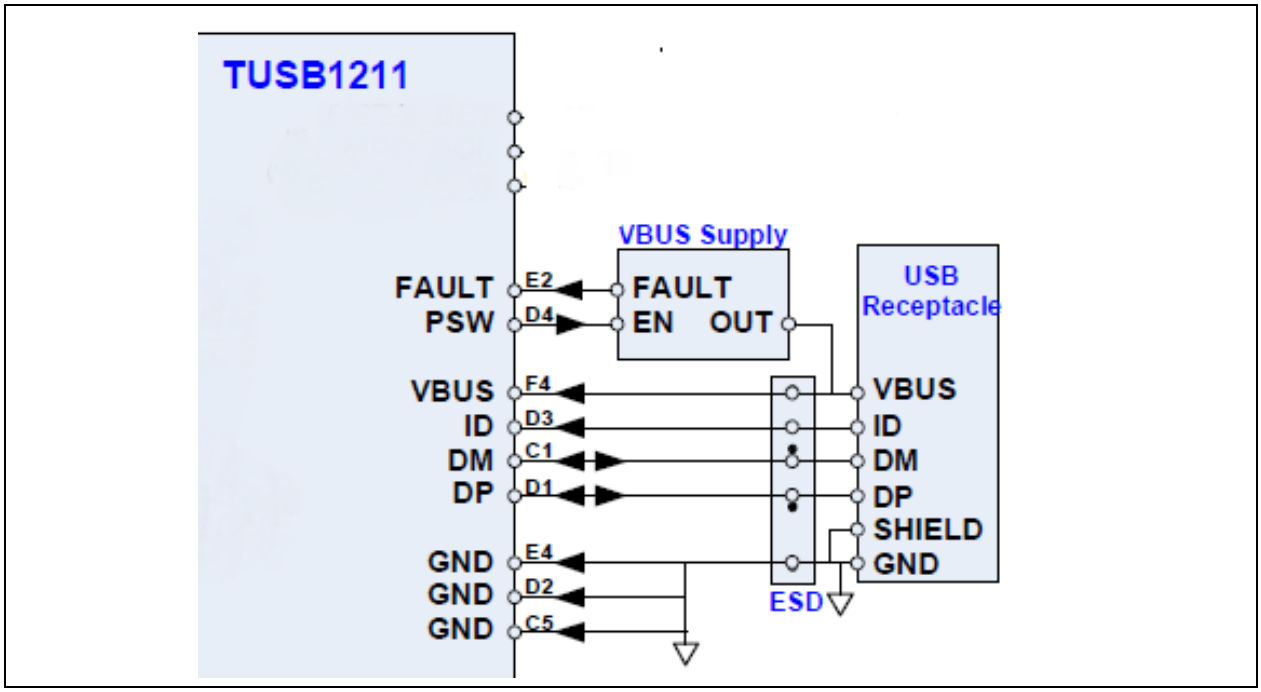
4.8 USB

The Edison module has a single USB 2.0 interface. This interface is the primary method for downloading code. The interface is found on pins: 3, 16, 18, and 20.

Note: The USB_VBUS signal should be applied to pin 20. This signal is only used to alert the Edison module that it has been connected to a host port.

The Edison module does not use power applied to pin 20 to power the device. Edison is designed to support OTG, using the ID signal on pin 3. The OTG power function is offboard. Two signals PSW (pin 21), and FAULT (pin 19) from the ULPI controller are used to control the external power switch and monitor the overcurrent condition on VBUS. Figure 4 shows the configuration of the **external hardware**.

Figure 4 Example Edison external USB design



The PSW signal is active high and controls an external VBUS power switch or charge pump.

The FAULT signal is active low. **FAULT should be connected to GND if USB host mode is not used.**

4.9 Clocks

Edison has two clock outputs. A 32 KHz sleep clock connected to pin 7 and a high frequency 19.2 MHz clock connected to pin 67. The sleep clock has +/-5mA drive capability, and may be programmed to provide an output when the SoC is in a sleep state. The high frequency 19.2 MHz clock has a drive strength of TBD mA. Buffering of the clocks may be necessary, depending on external trace lengths.

4.10 System reset

Edison has two system reset signals PWRBTN# (pin 17) and RESET_OUT# (pin 36). The PWRBTN# pin is an active low input which can cause the Edison module to transition into and out of sleep, or cause a power off , depending on the configuration of the software. RESET_OUT# is open-drain, and driven low by default out of system reset. This signal can be used by external hardware to indicate system reset. The Edison I/Os are undefined until RESET_OUT# transitions high.

4.11 Special software recovery

Edison has two signals used during boot, to cause the SoC to force firmware and OS image download and is useful to provide a recovery mechanism in the event of a corrupted flash image. These signals are FW_RCVR on pin 69, and RCVR_MODE on pin 31. The FW_RCVR signal must be held low during boot until RESET_OUT# goes high.

4.12 Power input and output

There are five power rails on the Edison module, VSYS, 3.3V, 1.8V, USB_VBUS, and V_VBAT_BKUP. VSYS is the only input power rail to the Edison module and the voltage range is 3.15V to 4.5V. USB_VBUS is a standard USB VBUS input from 4.75V to 5.25V. This rail is not used to power the device. It is only used by the USB ULPI PHY to determine a host device has attached to the Edison device. The 3.3V and 1.8V are power outputs from the Edison module that source a maximum of 250mA (TBV).

DCIN is a signal which indicates whether Edison is being power from a battery or from an external power source. DCIN also sets the voltage level required on VSYS in order to boot. When DCIN is floating or tied to ground the voltage on VSYS MUST rise from 2.5 to 3.5 V in 100 milliseconds, otherwise the boot is aborted. When the boot is aborted, power must be cycled below 2.5V. If DCIN is connected to VSYS, Edison will start to boot when VSYS is above 2.5 V for 100 milliseconds.

Note: The absolute minimum voltage to assure Wi-Fi and Bluetooth functionality is 3.15 V.

4.13 V_VBAT_BKUP

The PMIC has a dedicated charging subsystem for the backup supply, allowing the use of either rechargeable coin cell batteries or super-capacitors. The external cell should be connected to pin 23, V_VBAT_BKUP. The PMIC can be programmed with charge voltage of 2.5, 3.0, 3.15 or 3.3V. The charge current is programmable to 10, 50, 100, or 500uA. The default settings are 2.5V and 10uA. The capability to change these values is TBD.

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5 Powering Edison

Edison may be embedded in a number of devices either battery powered, or AC wall powered. Therefore, Edison was designed not to support a specific power delivery method or specific battery chemistry and capacity range. This portion of the design is left to the end user. With the interfaces available smart battery coulomb counters and smart rechargers could be placed onto one of the available I2C busses. Porting of the software to the specific bus would be the responsibility of the end user.

5.1 Main power supply VSYS

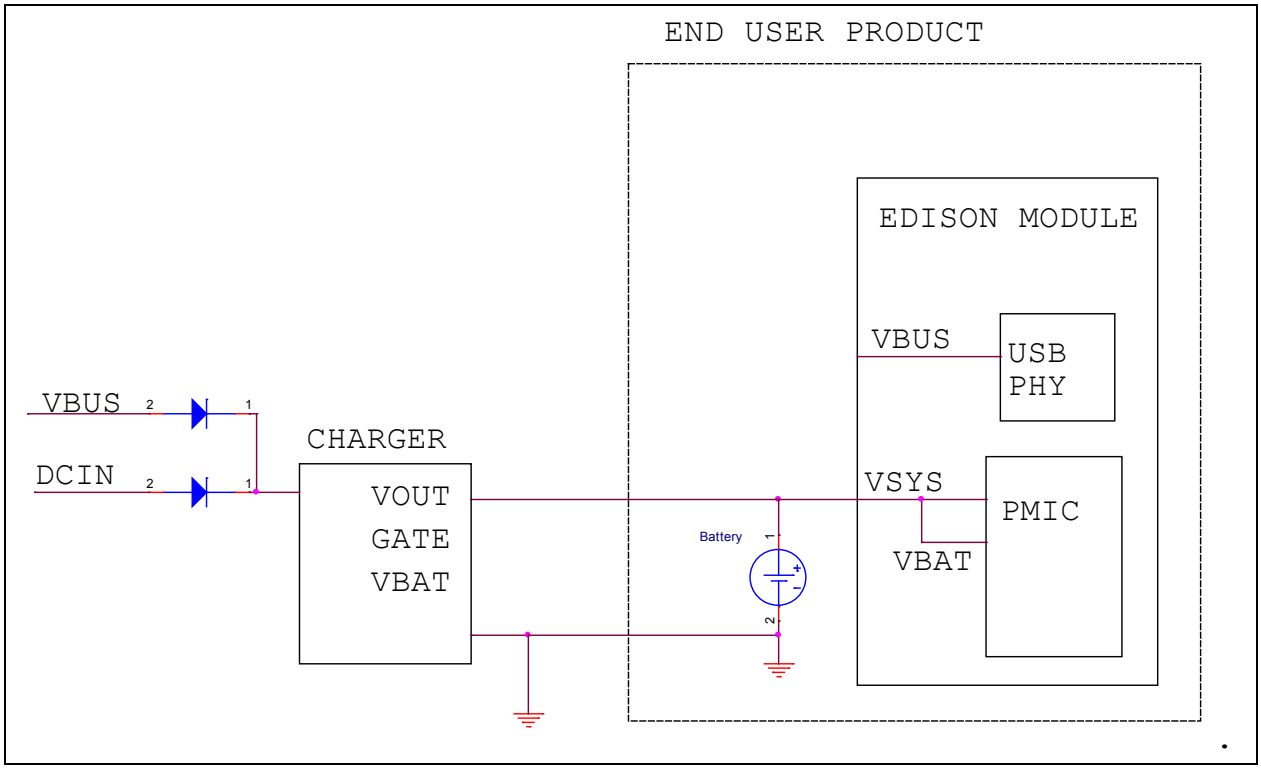
Edison uses VSYS (pins 2, 4, and 6) as the only power input path. Internal to Edison this signal is also connected to the VBAT path. Application of power to VSYS is interpreted as a battery insertion and will cause Edison to boot. The VSYS power range is 3.15V min to 4.5V max (see Section 4.12). This allows VSYS to run off a standard lithium ion battery. There are a number of possible power configurations for Edison, based on the size and cost sensitivity of the end user product.

5.2 Lithium-polymer battery direct attach

The simplest battery power connection to Edison is to directly attach a battery to VSYS, as shown in Figure 5. We do not recommend this configuration, however, as the charging system cannot distinguish between charge current and total system current.

Note: If Edison is prevented from booting by holding the power button signal PWRBTN# (pin 17) low, then the power input can be assumed to be the battery charging current.

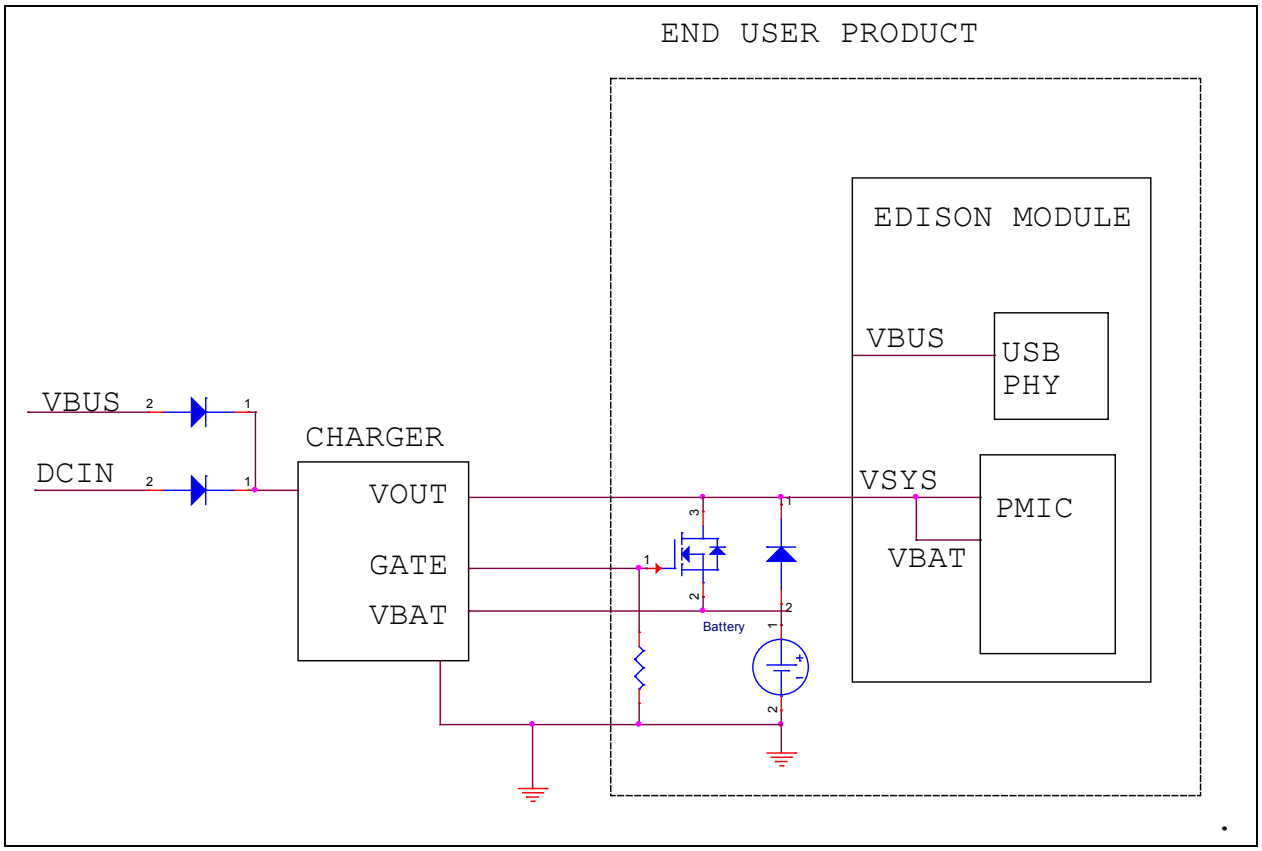
Figure 5 Example Edison lithium-polymer battery direct attach



5.3 Lithium-polymer battery with diode or FET isolation

In this configuration, Edison will see a diode drop during normal operation. This configuration allows the system to boot even with a dead battery. This configuration requires an additional pin to the external world to control the charging. Replacing the diode with a PFET, and pulling the gate low will remove the diode drop power loss. The external charger would require a gate control pin for an external PFET. This function is found on rechargers like BQ24073.

Figure 6 Example Edison lithium-polymer battery with FET isolation



5.4 Connection to USB VBUS

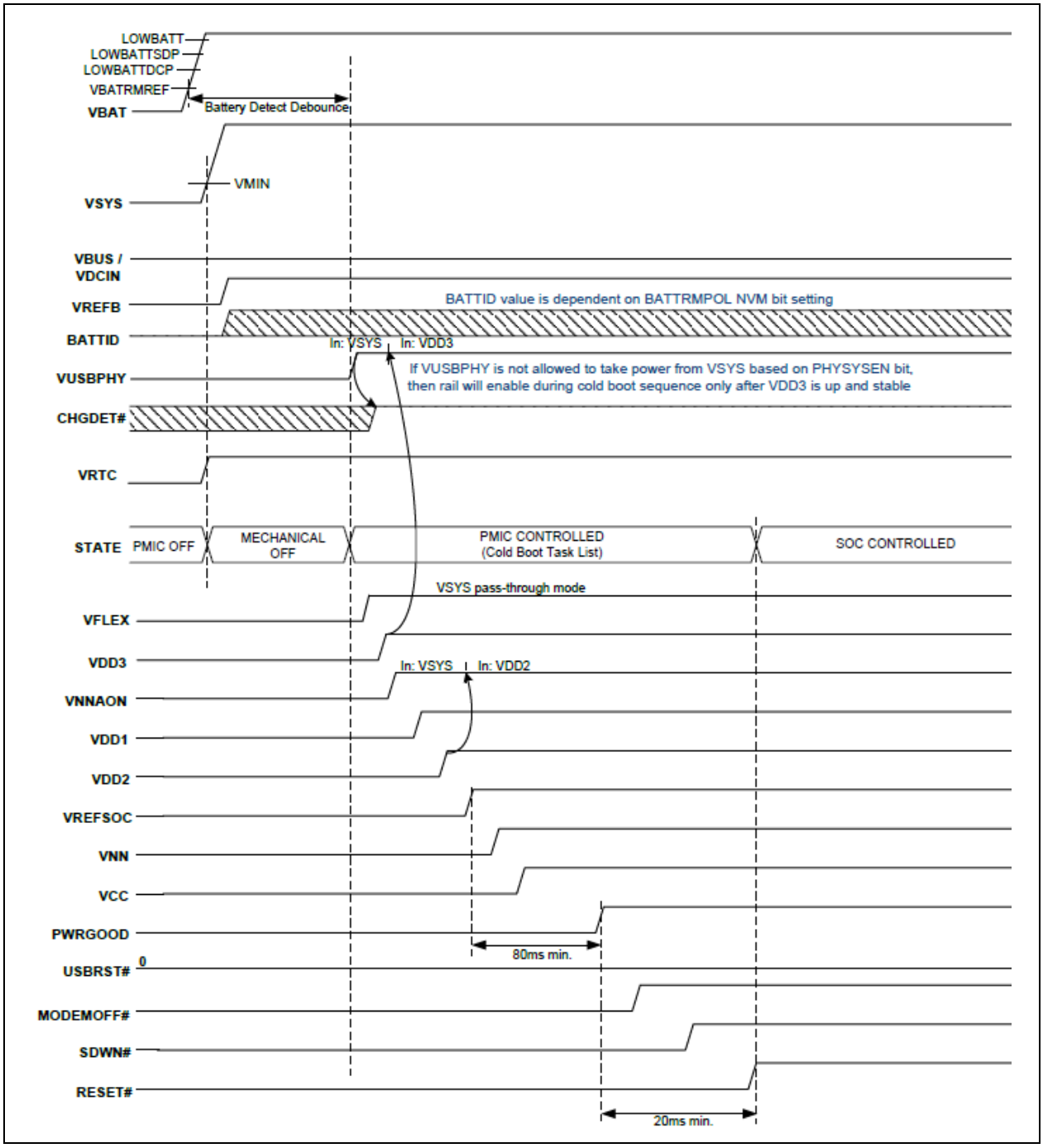
It is **NOT** possible to run Edison directly off a USB power supply. The maximum input voltage to VSYS should be less than 4.5V. The USB power supply specification (4.75V – 5.25V) exceeds the safe operational range of Edison. USB power must be down converted with an LDO or small buck switching converter or a recharger like BQ24074.

5.5 Cold boot sequence

Figure 6 shows the signal sequence from a cold boot.

Note: The reset# signal in Figure 6 is accessible on the 70-pin connectors as RESET_OUT# on pin 36.

Figure 7 Edison cold boot sequence



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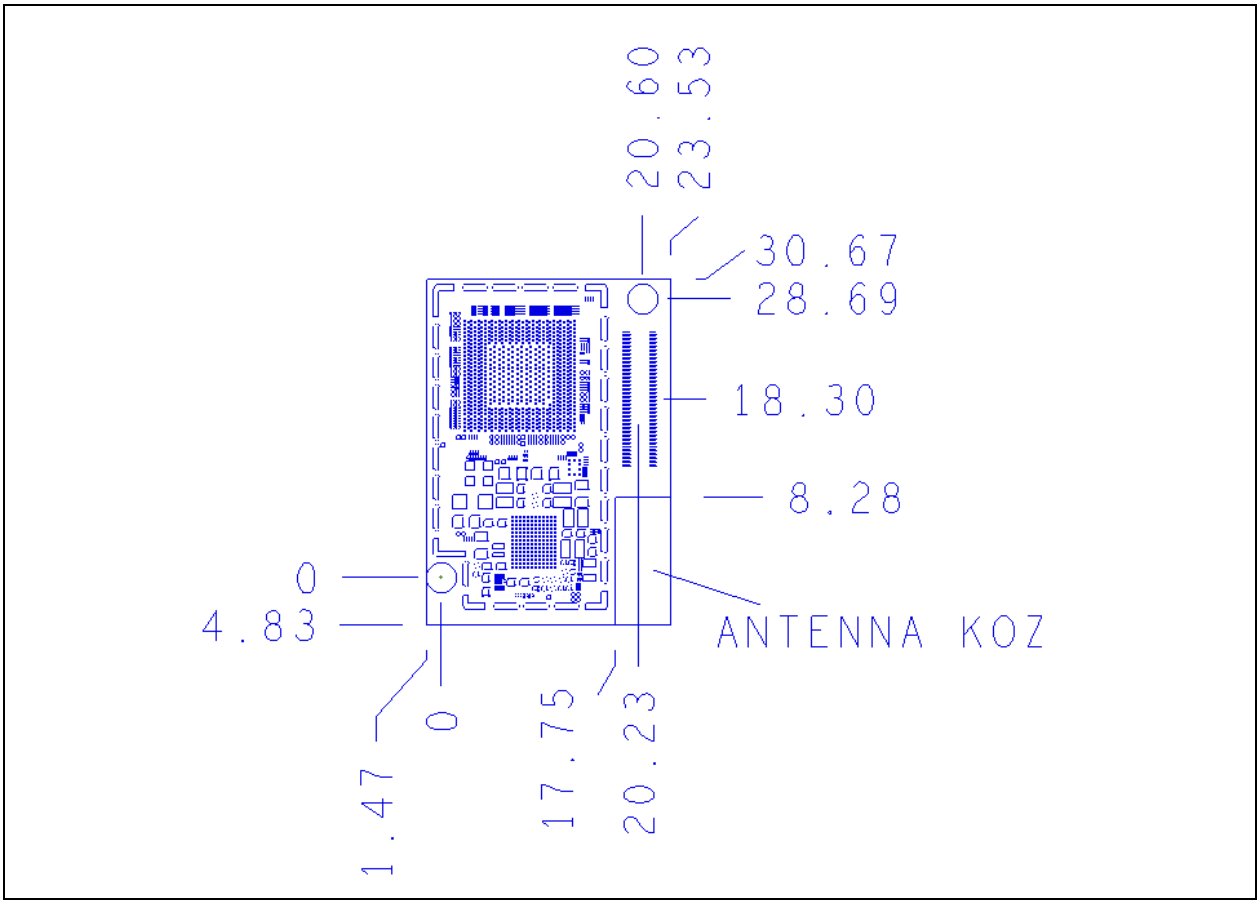
6 Edison Mechanicals

Figure 8 shows the dimensions (in millimeters) of the Edison module.

Figure 8 Edison mechanical dimensions (top view through PCB)



The location for pin 1 of the 70-pin connector is the lower right corner of the connector. The location of pin 2 is across the connector at the lower left corner. Consequently, the location of pin 69 is the upper right corner of the connector and the location of pin 70 is the upper left corner of the connector. The center point of the connector is specified in the drawing.

The diameters of the two mounting holes are 2.0 mm. Screw heads should be less than 3.0 mm. The mounting holes were designed for a T1.6 mm screw.

Note: The onboard chip antenna is in the lower right corner of Edison is denoted in the drawing as "ANTENNA KOZ". User-designed expansion PCBs should not place components or metallic objects close to the antenna keepout zone.

Most components on both sides of Edison will be covered with a shield. The height of the shields on both sides of the board, as measured from the surface of the PCB, is approximately 1.5 mm. The PCB thickness is specified as 0.8 mm ±0.1 mm. Therefore, the total maximum thickness of Edison is 3.9 mm. These values are verified with DVT modules.

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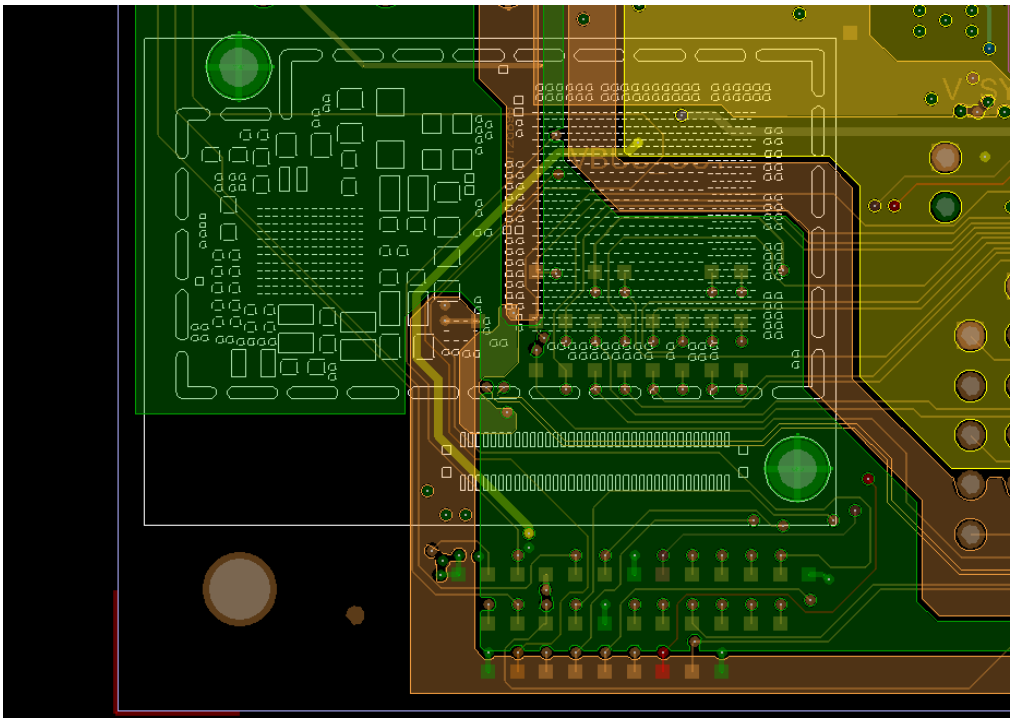
7 Layout

7.1 Antenna keepout

The area under and around the antenna should be kept free of all components, routes, and ground plane. The Intel® Edison board DXF in white with antenna keepout shown in the Arduino* trace layers. See Figure 9.

Figure 9 Area around antenna



7.2 Layout SD card, I2S, SPI, I2C

Table 8 Layout SD card

Signal parameter	Metric (mm)	Standard (mils)
Total length L1	0.254 to 101.6 mm	10 to 4000 mils
DATA/CMD/CTRL to CLK maximum pin-to-pin length mismatch	±2.54 mm	±100 mils
Minimum main route spacing ratio	60 × 60 µm. 1:1 trace width/space.	
CLK to DATA/CMD/CTRL matching	±200 mils	
Characteristic single ended impedance	42 to 45 ohm (±10%)	
Load capacitance	2 to 5 pF	

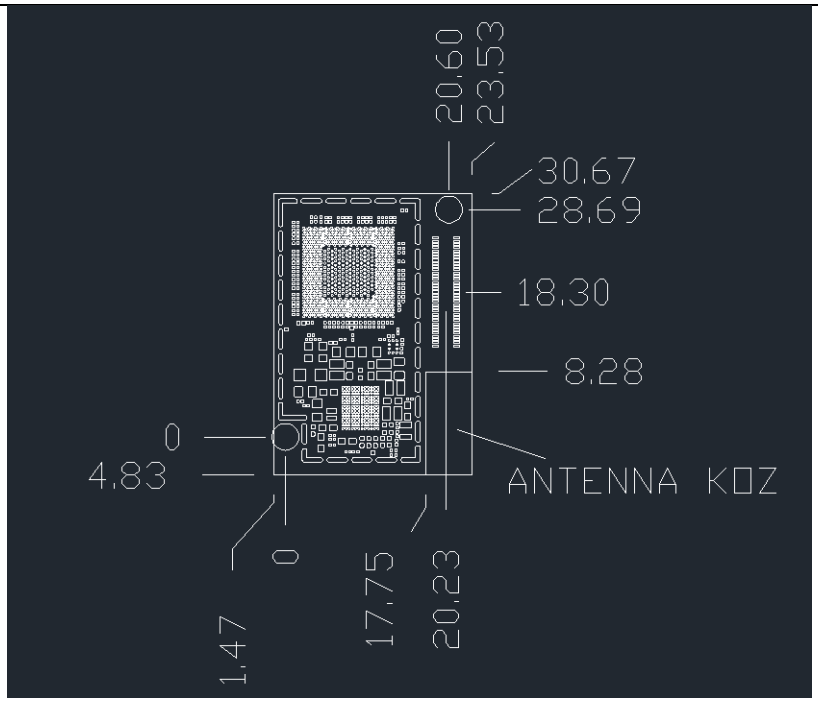
Note: 1) For SPI, total length is 6000 mils.
2) For I^2C, total length is 8000 mils.

7.3 Layout DXF

The following embedded file is a DXF of the Edison module as shown in the picture below.

Note: KOZ is keep out zone.

Figure 10 Layout DXF

Package (See attachment: *Edison_DVT.dxf*)	

7.4 Layout PTC EMN files

Figure 11 PTC EMN graphic

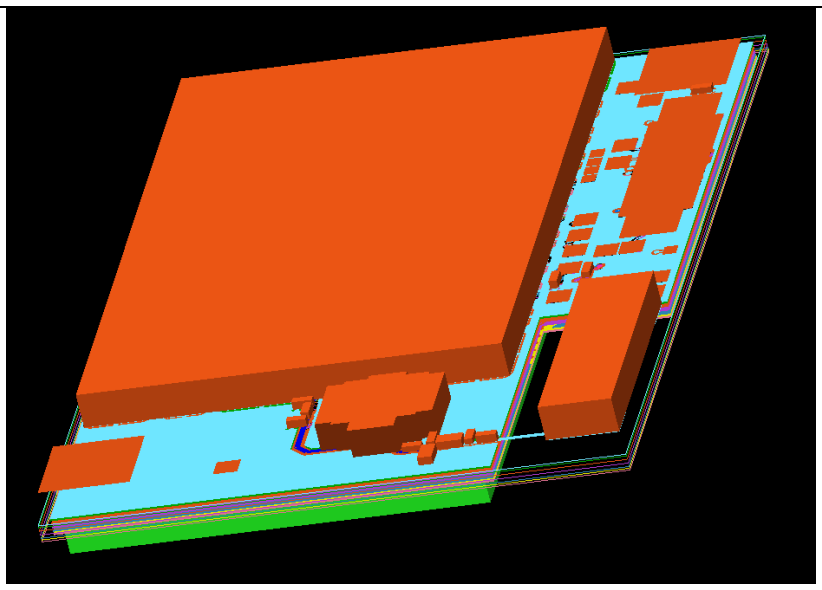
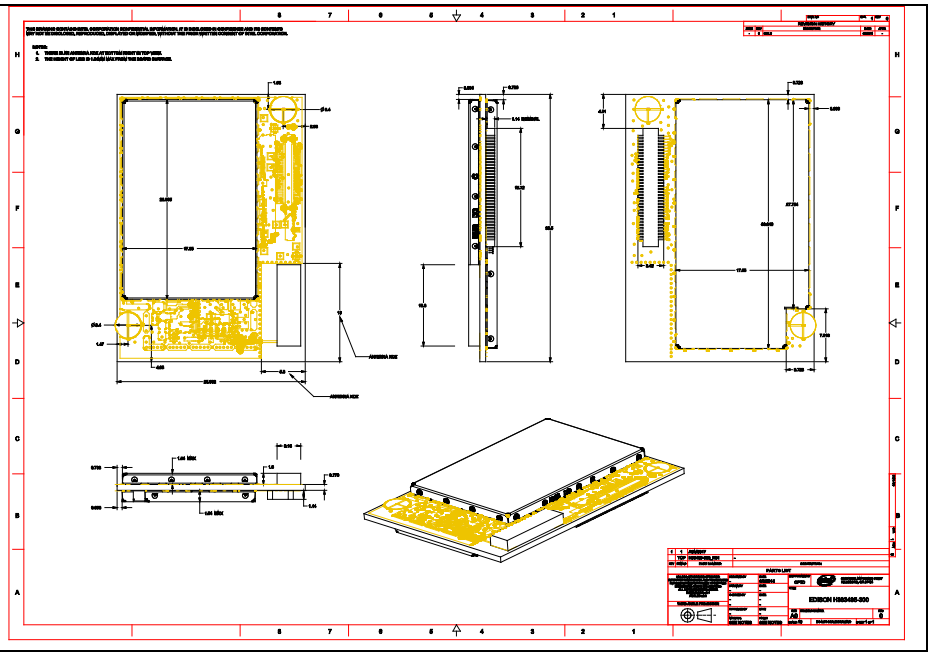
H38489-005_R02 _emn.emn (See attachment: *H38489-005_R02 _emn.emn*)	
H38489-005_R02 _emn.emp (See attachment: *H38489-005_R02 _emn.emp*)	

Figure 12 EDISON H383485-300

Adobe Acrobat Document

(See attachment: *H383485-300.pdf*)



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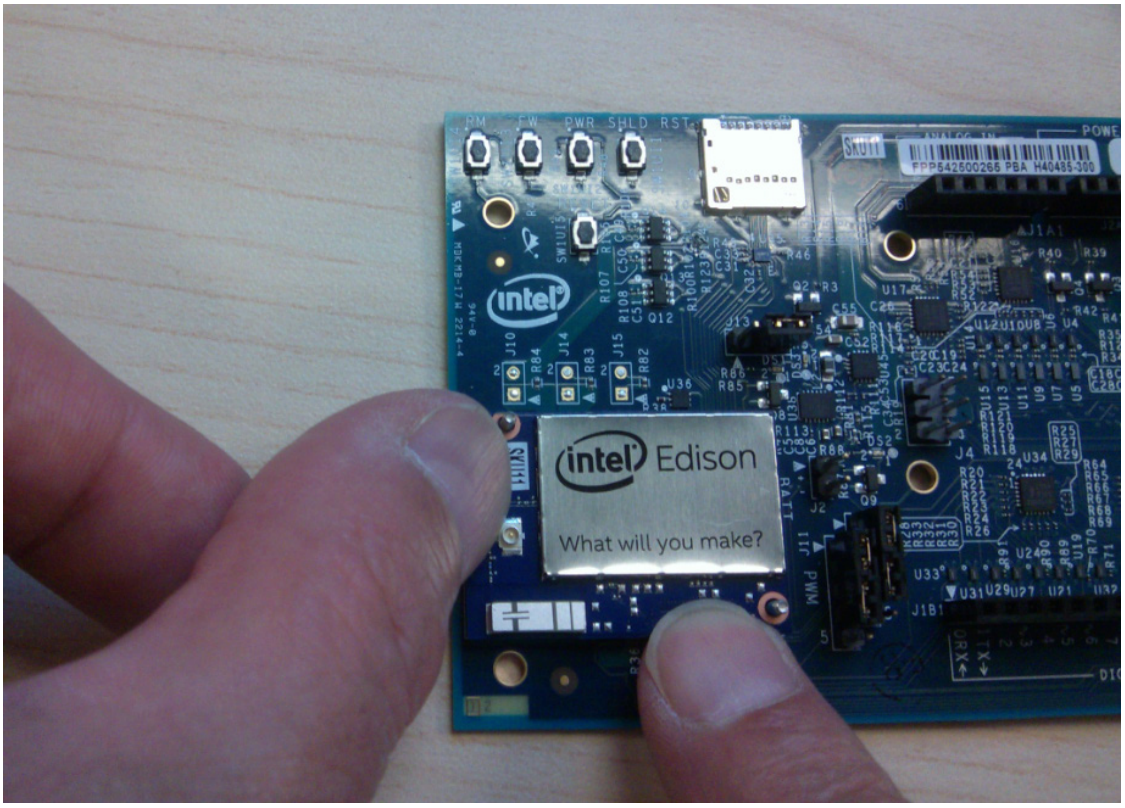
8 Handling

When assembling an Intel® Edison module to an Arduino board, handle the Intel® Edison module by the PCB edges. Avoid holding or exerting pressure to the shields. To mate the Intel® Edison board to the Arduino* board, apply pressure directly above the connector and to the left corner, as shown in Figure 13.

Figure 13 Inserting an Edison module



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9 Debug UART Errata

The Intel® Edison board has a known error on all UARTs. When Edison goes into low power sleep, the UART internal FIFO and interface is powered down. Therefore, a two-wire UART (Rx/Tx) will lose the first received character whenever Edison is in sleep mode. In order to avoid this condition, when sleep mode is enabled, a four-wire UART (Rx, Tx, CTS, and RTS) is required.

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