



MICROCHIP dsPIC33EPXXXGS70X/80X FAMILY

16-Bit Digital Signal Controllers for Digital Power Applications with Interconnected High-Speed PWM, ADC, PGA and Comparators

Operating Conditions

- 3.0V to 3.6V, -40°C to +85°C, DC to 70 MIPS
- 3.0V to 3.6V, -40°C to +125°C, DC to 60 MIPS

Flash Architecture

- Dual Partition Flash Program Memory with Live Update:
 - Supports programming while operating
 - Supports partition soft swap

Core: 16-Bit dsPIC33E CPU

- Code-Efficient (C and Assembly) Architecture
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support
- Four Additional Working Register Sets (reduces context switching)

Clock Management

- $\pm 0.9\%$ Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 0.5 mA/MHz Dynamic Current (typical)
- 20 μ A IPD Current (typical)

High-Speed PWM

- Eight PWM Generators (two outputs per generator)

Advanced Analog Features

- High-Speed ADC module:
 - 12-bit with 4 dedicated SAR ADC cores and one shared SAR ADC core
 - Configurable resolution (up to 12-bit) for each ADC core
 - Up to 3.25 Msps conversion rate per channel at 12-bit resolution
 - 11 to 22 single-ended inputs
 - Dedicated result buffer for each analog channel
 - Flexible and independent ADC trigger sources
 - Two digital comparators
 - Two oversampling filters for increased resolution
- Four Rail-to-Rail Comparators with Hysteresis:
 - Dedicated 12-bit Digital-to-Analog Converter (DAC) for each analog comparator
 - Up to two DAC reference outputs
 - Up to two external reference inputs
- Two Programmable Gain Amplifiers:
 - Single-ended or independent ground reference
 - Five selectable gains (4x, 8x, 16x, 32x and 64x)
 - 40 MHz gain bandwidth

Interconnected SMPS Peripherals

- Reduces CPU Interaction to Improve Performance
- Flexible PWM Trigger Options for ADC Conversions
- High-Speed Comparator Truncates PWM (15 ns typical):
 - Supports Cycle-by-Cycle Current mode control
 - Current Reset mode (variable frequency)

Timers/Output Compare/Input Capture

- Five 16-Bit and up to Two 32-Bit Timers/Counters

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Communication Interfaces

- Two UART modules (15 Mbps):
 - Supports LIN/J2602 protocols and IrDA®
- Three Variable Width SPI modules with Operating modes:
 - 3-wire SPI
 - 8x16 or 8x8 FIFO mode
 - I²S mode
- Two I²C modules (up to 1 Mbaud) with SMBus Support
- Up to Two CAN modules
- Four-Channel DMA

Input/Output

- Constant-Current Source (10 µA nominal)
- Sink/Source up to 12 mA/15 mA, respectively; Pin-Specific for Standard VOH/VOL
- 5V Tolerant Pins
- Selectable, Open-Drain Pull-ups and Pull-Downs
- External Interrupts on all I/O Pins
- Peripheral Pin Select (PPS) to allow Function Remap with Six Virtual I/Os

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C)
- Class B Safety Library, IEC 60730
- The 6x6x0.55 mm UQFN Package is Designed and Optimized to ease IPC9592B 2nd Level Temperature Cycle Qualification

Debugger Development Support

- In-Circuit and In-Application Programming
- Five Program and Three Complex Data Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

Digital Peripherals

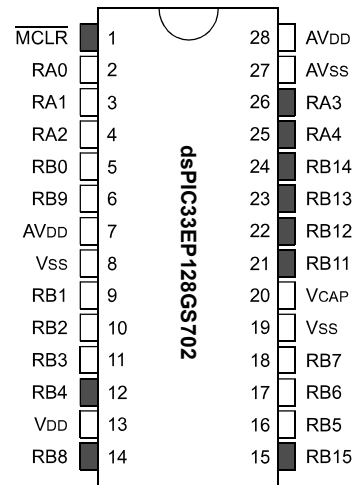
- Four Configurable Logic Cells
- Peripheral Trigger Generator

Device	Pins	Program Memory Bytes	RAM (Bytes)	General Purpose I/O (GPIO)	Remappable Peripherals										12-Bit ADC		PGA	DMA	Analog Comparator	DAC Output	Constant-Current Source	Packages		
					Timers ⁽¹⁾	Input Capture	Output Compare	UART	SPI	PWM ⁽²⁾	External Interrupts ⁽³⁾	CAN	Reference Clock	I ² C	CLC	PTG							Analog Inputs	S&H Circuits
dsPIC33EP128GS702	28	128K	8K	20	5	4	4	2	3	8x2	4	0	1	2	4	1	11	5	2	0	4	1	1	SOIC, QFN-S, UQFN
dsPIC33EP64GS804	44	64K	8K	33	5	4	4	2	3	8x2	4	2	1	2	4	1	17	5	2	4	4	1	1	QFN, TQFP
dsPIC33EP128GS704	44	128K	8K	33	5	4	4	2	3	8x2	4	0	1	2	4	1	17	5	2	0	4	1	1	
dsPIC33EP128GS804	44	128K	8K	33	5	4	4	2	3	8x2	4	2	1	2	4	1	17	5	2	4	4	1	1	
dsPIC33EP64GS805	48	64K	8K	33	5	4	4	2	3	8x2	4	2	1	2	4	1	17	5	2	4	4	1	1	TQFP
dsPIC33EP128GS705	48	128K	8K	33	5	4	4	2	3	8x2	4	0	1	2	4	1	17	5	2	0	4	1	1	
dsPIC33EP128GS805	48	128K	8K	33	5	4	4	2	3	8x2	4	2	1	2	4	1	17	5	2	4	4	1	1	
dsPIC33EP64GS806	64	64K	8K	51	5	4	4	2	3	8x2	4	2	1	2	4	1	22	5	2	4	4	2	1	

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Pin Diagrams

28-Pin SOIC



Pin	Pin Function	Pin	Pin Function
1	MCLR	15	PGEC3/SCL2/RP47/RB15
2	AN0/CMP1A/PGA1P1/RP16/RA0	16	TDO/AN19/PGA2N2/RP37/RB5
3	AN1/CMP1B/PGA1P2/PGA2P1/RP17/RA1	17	PGED1/TDI/AN20/SCL1/RP38/RB6
4	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/RP18/RA2	18	PGEC1/AN21/SDA1/RP39/RB7
5	AN3/CMP1D/CMP2B/PGA2P3/RP32/RB0	19	VSS
6	AN4/CMP2C/CMP3A/ISRC4/RP41/RB9	20	VCAP
7	AVDD	21	TMS/PWM3H/RP43/RB11
8	VSS	22	TCK/PWM3L/RP44/RB12
9	OSCI/CLKI/AN6/CMP3C/CMP4A/ISRC2/RP33/RB1	23	PWM2H/RP45/RB13
10	OSC2/CLKO/AN7/CMP3D/CMP4B/PGA1N2/RP34/RB2	24	PWM2L/RP46/RB14
11	PGED2/DACOUT1/AN18/INT0/RP35/RB3	25	PWM1H/RP20/RA4
12	PGEC2/ADTRG31/EXTREF1/RP36/RB4	26	PWM1L/RP19/RA3
13	VDD	27	AVSS
14	PGED3/SDA2/FLT31/RP40/RB8	28	AVDD

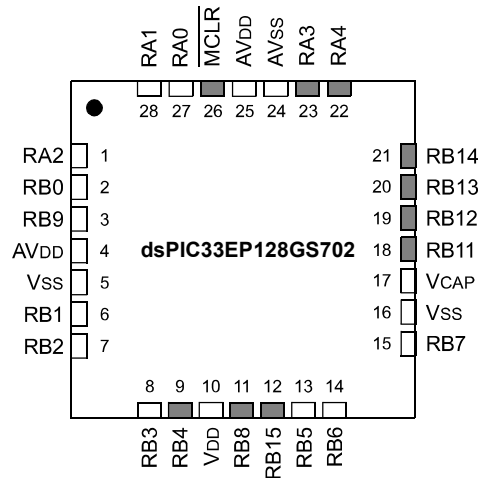
Legend: Shaded pins are up to 5 VDC tolerant.

RPn represents remappable peripheral functions. See [Table 11-12](#) and [Table 11-13](#) for the complete list of remappable sources.

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Pin Diagrams (Continued)

28-Pin QFN-S, UQFN

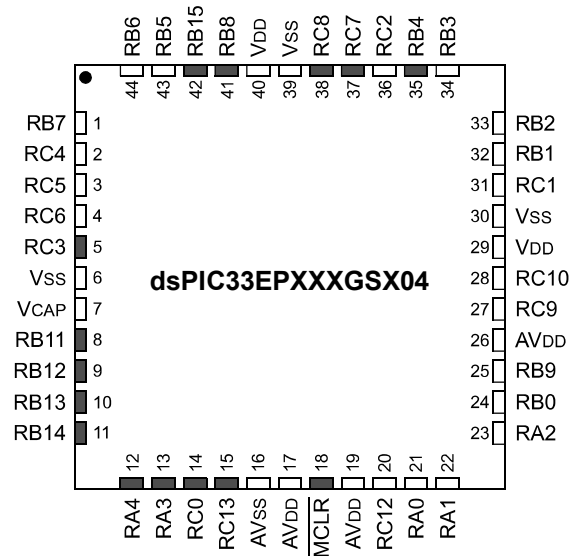


Pin	Pin Function	Pin	Pin Function
1	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/ RP18 /RA2	15	PGEC1/AN21/SDA1/ RP39 /RB7
2	AN3/CMP1D/CMP2B/PGA2P3/ RP32 /RB0	16	VSS
3	AN4/CMP2C/CMP3A/ISRC4/ RP41 /RB9	17	VCAP
4	AVDD	18	TMS/PWM3H/ RP46 /RB11
5	VSS	19	TCK/PWM3L/ RP44 /RB12
6	OSCI/CLKI/AN6/CMP3C/CMP4A/ISRC2/ RP33 /RB1	20	PWM2H/ RP45 /RB13
7	OSC2/CLKO/AN7/CMP3D/CMP4B/PGA1N2/ RP34 /RB2	21	PWM2L/ RP46 /RB14
8	PGED2/DACOUT1/AN18/INT0/ RP35 /RB3	22	PWM1H/ RP20 /RA4
9	PGEC2/ADTRG31/EXTREF1/ RP36 /RB4	23	PWM1L/ RP19 /RA3
10	VDD	24	AVSS
11	PGED3/SDA2/FLT31/ RP40 /RB8	25	AVDD
12	PGEC3/SCL2/ RP47 /RB15	26	MCLR
13	TDO/AN19/PGA2N2/ RP37 /RB5	27	AN0/CMP1A/PGA1P1/ RP16 /RA0
14	PGED1/TDI/AN20/SCL1/ RP38 /RB6	28	AN1/CMP1B/PGA1P2/PGA2P1/ RP17 /RA1

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Pin Diagrams (Continued)

44-Pin QFN, TQFP

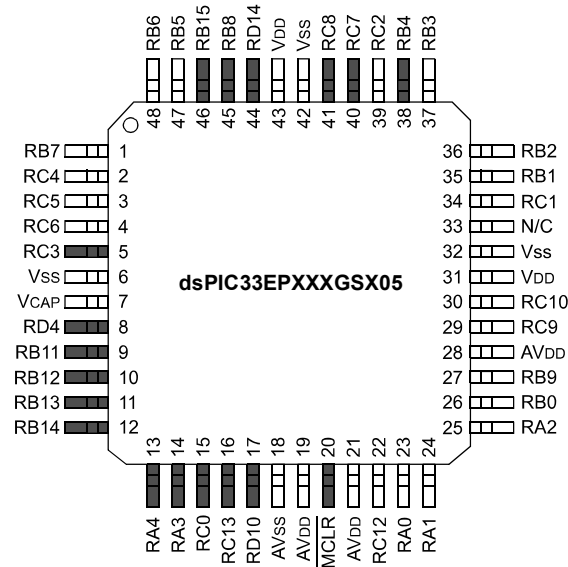


Pin	Pin Function	Pin	Pin Function
1	PGEC1/AN21/SDA1/RP39/RB7	23	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/RP18/RA2
2	AN1ALT/RP52/RC4	24	AN3/CMP1D/CMP2B/PGA2P3/RP32/RB0
3	AN0ALT/RP53/RC5	25	AN4/CMP2C/CMP3A/ISRC4/RP41/RB9
4	AN17/RP54/RC6	26	AVDD
5	RP51/RC3	27	AN11/PGA1N3/RP57/RC9
6	Vss	28	EXTREF2/AN10/PGA1P4/RP58/RC10
7	VCAP	29	VDD
8	TMS/PWM3H/RP43/RB11	30	Vss
9	TCK/PWM3L/RP44/RB12	31	AN8/CMP4C/PGA2P4/RP49/RC1
10	PWM2H/RP45/RB13	32	OSCI/CLKI/AN6/CMP3C/CMP4A/ISRC2/RP33/RB1
11	PWM2L/RP46/RB14	33	OSC2/CLKO/AN7/CMP3D/CMP4B/PGA1N2/RP34/RB2
12	PWM1H/RP20/RA4	34	PGED2/DACOUT1/AN18/INT0/RP35/RB3
13	PWM1L/RP19/RA3	35	PGEC2/ADTRG31/RP36/RB4
14	FLT12/RP48/RC0	36	EXTREF1/AN9/CMP4D/RP50/RC2
15	FLT11/RP61/RC13	37	ASDA1/RP55/RC7
16	AVss	38	ASCL1/RP56/RC8
17	AVDD	39	Vss
18	MCLR	40	VDD
19	AVDD	41	PGED3/SDA2/FLT31/RP40/RB8

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Pin Diagrams (Continued)

48-Pin TQFP

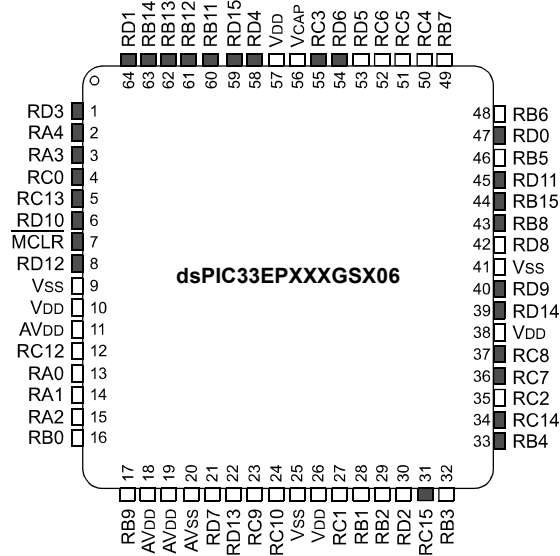


Pin	Pin Function	Pin	Pin Function
1	PGEC1/AN21/SDA1/RP39/RB7	25	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/RP18/RA2
2	AN1ALT/RP52/RC4	26	AN3/CMP1D/CMP2B/PGA2P3/RP32/RB0
3	AN0ALT/RP53/RC5	27	AN4/CMP2C/CMP3A/ISRC4/RP41/RB9
4	AN17/RP54/RC6	28	AVDD
5	RP51/RC3	29	AN11/PGA1N3/RP57/RC9
6	Vss	30	EXTREF2/AN10/PGA1P4/RP58/RC10
7	VCAP	31	VDD
8	RP68/RD4	32	Vss
9	TMS/PWM3H/RP43/RB11	33	N/C
10	TCK/PWM3L/RP44/RB12	34	AN8/CMP4C/PGA2P4/RP49/RC1
11	PWM2H/RP45/RB13	35	OSCI/CLKI/AN6/CMP3C/CMP4A/ISRC2/RP33/RB1
12	PWM2L/RP46/RB14	36	OSC2/CLKO/AN7/CMP3D/CMP4B/PGA1N2/RP34/RB2
13	PWM1H/RP20/RA4	37	PGED2/DACOUT1/AN18/INT0/RP35/RB3
14	PWM1L/RP19/RA3	38	PGEC2/ADTRG31/RP36/RB4
15	FLT12/RP48/RC0	39	EXTREF1/AN9/CMP4D/RP50/RC2
16	FLT11/RP61/RC13	40	ASDA1/RP55/RC7
17	CLC4OUT/FLT10/RP74/RD10	41	ASCL1/RP56/RC8
18	AVss	42	Vss
19	AVDD	43	VDD
20	MCLR	44	CLC2OUT/RD14

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Pin Diagrams (Continued)

64-Pin TQFP

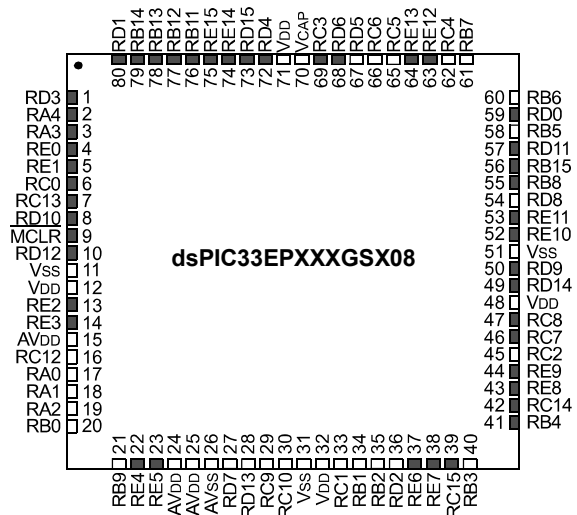


Pin	Pin Function	Pin	Pin Function
1	PWM4L/ RP67 /RD3	33	PGEC2/ADTRG31/ RP36 /RB4
2	PWM1H/ RP20 /RA4	34	RP62 /RC14
3	PWM1L/ RP19 /RA3	35	EXTREF1/AN9/CMP4D/ RP50 /RC2
4	FLT12/ RP48 /RC0	36	ASDA1/ RP55 /RC7
5	FLT11/ RP61 /RC13	37	ASCL1/ RP56 /RC8
6	CLC4OUT/FLT10/ RP74 /RD10	38	VDD
7	MCLR	39	CLC3OUT/RD14
8	T5CK/FLT9/ RP76 /RD12	40	SCK3/ RP73 /RD9
9	Vss	41	Vss
10	VDD	42	AN5/CMP2D/CMP3B/ISRC3/ RP72 RD8
11	AVDD	43	PGED3/SDA2/FLT31/ RP40 /RB8
12	AN14/PGA2N3/ RP60 /RC12	44	PGEC3/SCL2/ RP47 /RB15
13	AN0/CMP1A/PGA1P1/ RP16 /RA0	45	INT4/ RP75 /RD11
14	AN1/CMP1B/PGA1P2/PGA2P1/ RP17 /RA1	46	TDO/AN19/PGA2N2/ RP37 /RB5
15	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/ RP18 /RA2	47	T4CK/ RP64 /RD0
16	AN3/CMP1D/CMP2B/PGA2P3/ RP32 /RB0	48	PGED1/TDI/AN20/SCL1/ RP38 /RB6
17	AN4/CMP2C/CMP3A/ISRC4/ RP41 /RB9	49	PGEC1/AN21/SDA1/ RP39 /RB7
18	AVDD	50	AN1ALT/ RP52 /RC4
19	AVDD	51	AN0ALT/ RP53 /RC5
20	AVss	52	AN17/ RP54 /RC6
21	AN15/ RP71 /RD7	53	AN12/ISRC1/ RP69 /RD5
22	DACOUT2/AN13/RD13	54	PWM5H/ RP70 /RD6
23	AN11/PGA1N3/ RP57 /RC9	55	PWM5L/ RP51 /RC3
24	EXTREF2/AN10/PGA1P4/ RP58 /RC10	56	VCAP

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Pin Diagrams (Continued)

80-Pin TQFP



Pin	Pin Function	Pin	Pin Function
1	PWM4L/RP67/RD3	41	PGEC2/ADTRG31/RP36/RB4
2	PWM1H/RP20/RA4	42	RP62/RC14
3	PWM1L/RP19/RA3	43	RE8
4	PWM8L/RE0	44	RE9
5	PWM8H/RE1	45	EXTREF1/AN9/CMP4D/RP50/RC2
6	FLT12/RP48/RC0	46	ASDA1/RP55/RC7
7	FLT11/RP61/RC13	47	ASCL1/RP56/RC8
8	CLC4OUT/FLT10/RP74/RD10	48	VDD
9	MCLR	49	CLC3OUT/RD14
10	T5CK/FLT9/RP76/RD12	50	SCK3/RP73/RD9
11	Vss	51	Vss
12	VDD	52	FLT21/RE10
13	FLT17/RE2	53	FLT22/RE11
14	FLT18/RE3	54	AN5/CMP2D/CMP3B/ISRC3/RP72/RD8
15	AVDD	55	PGED3/SDA2/FLT31/RP40/RB8
16	AN14/PGA2N3/RP60/RC12	56	PGEC3/SCL2/RP47/RB15
17	AN0/CMP1A/PGA1P1/RP16/RA0	57	INT4/RP75/RD11
18	AN1/CMP1B/PGA1P2/PGA2P1/RP17/RA1	58	TD0/AN19/PGA2N2/RP37/RB5
19	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/RP18/RA2	59	T4CK/RP64/RD0
20	AN3/CMP1D/CMP2B/PGA2P3/RP32/RB0	60	PGED1/TDI/AN20/SCL1/RP38/RB6
21	AN4/CMP2C/CMP3A/ISRC4/RP41/RB9	61	PGEC1/AN21/SDA1/RP39/RB7
22	RE4	62	AN1ALT/RP52/RC4
23	RE5	63	RE12
24	AVDD	64	RE13
25	AVDD	65	AN0ALT/RP53/RC5
26	AVss	66	AN17/RP54/RC6
27	AN15/RP71/RD7	67	AN12/ISRC1/RP69/RD5
28	DACOUT2/AN13/RD13	68	PWM5H/RP70/RD6
29	AN11/PGA1N3/RP57/RC9	69	PWM5L/RP51/RC3
30	EXTREF2/AN10/PGA1P4/RP58/RC10	70	VCAP
31	Vss	71	VDD

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1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

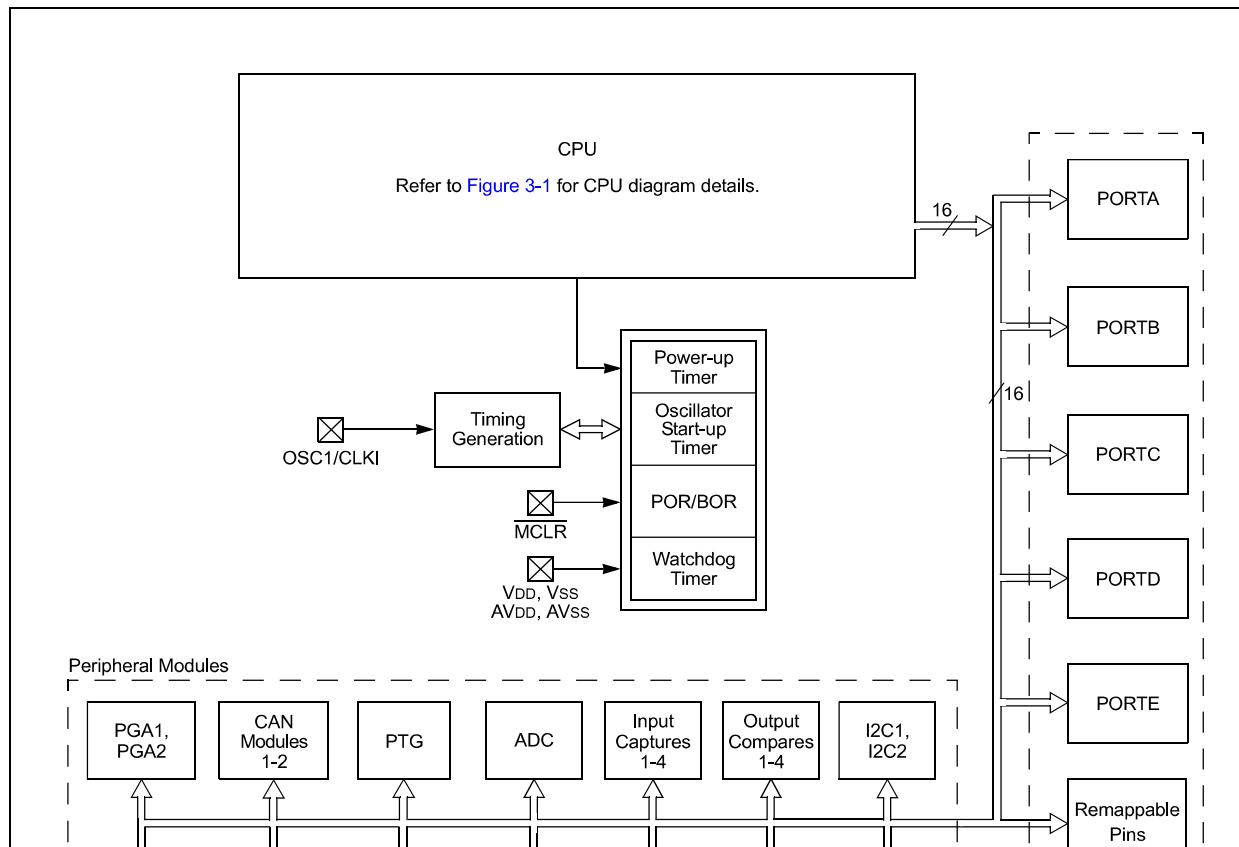
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGS70X/80X Digital Signal Controller (DSC) devices.

dsPIC33EPXXXGS70X/80X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGS70X/80X FAMILY BLOCK DIAGRAM



dsPIC33EPXXXGS70X/80X FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name ⁽¹⁾	Pin Type	Buffer Type	PPS	Description
AN0-AN21 AN0ALT-AN1ALT	I I	Analog Analog	No No	Analog input channels. Alternate analog input channels.
C1RXR C2RXR C1TX C2TX	I I O O	ST ST ST ST	Yes Yes Yes Yes	CAN1 receive. CAN2 receive. CAN1 transmit. CAN2 transmit.
CLKI CLKO	I O	ST/ CMOS —	No No	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1 OSC2	I I/O	ST/ CMOS —	No No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
CLC1OUT CLC2OUT CLC3OUT CLC4OUT	O O O O	DIG DIG DIG DIG	Yes Yes No ⁽⁴⁾ No ⁽⁴⁾	CLC1 output. CLC2 output. CLC3 output. CLC4 output.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 through 4.
OCFA OC1-OC4	I O	ST —	Yes Yes	Compare Fault A input (for compare channels). Compare Outputs 1 through 4.
INT0 INT1 INT2 INT4	I I I I	ST ST ST ST	No Yes Yes Yes	External Interrupt 0. External Interrupt 1. External Interrupt 2. External Interrupt 4.
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	No	PORTD is a bidirectional I/O port.
RE0-RE15	I/O	ST	No	PORTE is a bidirectional I/O port.
T1CK T2CK T3CK T4CK T5CK	I I I I I	ST ST ST ST ST	Yes Yes Yes No No	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input.
$\overline{U1CTS}$ $\overline{U1RTS}$ U1RX U1TX	I O I O	ST — ST —	Yes Yes Yes Yes	UART1 Clear-to-Send. UART1 Ready-to-Send. UART1 receive. UART1 transmit.

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name ⁽¹⁾	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	Yes	UART2 Clear-to-Send.
U2RTS	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
BCLK2	O	ST	Yes	UART2 IrDA baud clock output.
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	Yes	SPI1 data in.
SDO1	O	—	Yes	SPI1 data out.
SS1	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCK3	I/O	ST	Yes ⁽³⁾	Synchronous serial clock input/output for SPI3.
SDI3	I	ST	Yes	SPI3 data in.
SDO3	O	—	Yes	SPI3 data out.
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
FLT1-FLT8	I	ST	Yes	PWM Fault Inputs 1 through 8.
FLT9-FLT12	I	ST	No	PWM Fault Inputs 9 through 12.
PWM1L-PWM3L	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H	O	—	No	PWM High Outputs 1 through 3.
PWM4L-PWM8L ⁽²⁾	O	—	Yes	PWM Low Outputs 4 through 8.
PWM4H-PWM8H ⁽²⁾	O	—	Yes	PWM High Outputs 4 through 8.
SYNCI1, SYNCI2	I	ST	Yes	PWM Synchronization Inputs 1 and 2.
SYNCO1, SYNCO2	O	—	Yes	PWM Synchronization Outputs 1 and 2.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

1: Not all pins are available in all package variants. See the “Pin Diagrams” section for pin availability.

2: PWM4H/L through PWM8H/L are fixed on dsPIC33EPXXXGS708/808 devices. PWM4H/L through PWM6H/L are fixed on dsPIC33EPXXXGS706/806 devices.

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name ⁽¹⁾	Pin Type	Buffer Type	PPS	Description
CMP1A-CMP4A	I	Analog	No	Comparator Channels 1A through 4A inputs.
CMP1B-CMP4B	I	Analog	No	Comparator Channels 1B through 4B inputs.
CMP1C-CMP4C	I	Analog	No	Comparator Channels 1C through 4C inputs.
CMP1D-CMP4D	I	Analog	No	Comparator Channels 1D through 4D inputs.
ACMP1-ACMP4	O	—	Yes	Analog Comparator Outputs 1-4.
DACOUT1, DACOUT2	O	—	No	DAC Output Voltages 1 and 2.
EXTREF1, EXTREF2	I	Analog	No	External Voltage Reference Inputs 1 and 2 for the Reference DACs.
PGA1P1-PGA1P4	I	Analog	No	PGA1 Positive Inputs 1 through 4.
PGA1N1-PGA1N3	I	Analog	No	PGA1 Negative Inputs 1 through 3.
PGA2P1-PGA2P4	I	Analog	No	PGA2 Positive Inputs 1 through 4.
PGA2N1-PGA2N3	I	Analog	No	PGA2 Negative Inputs 1 through 3.
ADTRG31	I	ST	No	External ADC trigger source.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 PPS = Peripheral Pin Select TTL = TTL input buffer

- 1: Not all pins are available in all package variants. See the **“Pin Diagrams”** section for pin availability.
- 2: PWM4H/L through PWM8H/L are fixed on dsPIC33EPXXXGS708/808 devices. PWM4H/L through PWM6H/L are fixed on dsPIC33EPXXXGS706/806 devices.
- 3: The SCK3 pin is fixed on dsPIC33EPXXXGS706/806 and dsPIC33EPXXXGS708/808 devices.
- 4: PPS is available on dsPIC33EPXXXGS702 devices only.

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2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

- Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).
- 2:** Some registers and associated bits described in this section may not be available on all devices. Refer to [Section 4.0 “Memory Organization”](#) in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGS70X/80X family requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names which must always be connected:

- All VDD and VSS pins (see [Section 2.2 “Decoupling Capacitors”](#))
- All AVDD and AVSS pins regardless if ADC module is not used (see [Section 2.2 “Decoupling Capacitors”](#))
- VCAP (see [Section 2.3 “CPU Logic Filter Capacitor Connection \(VCAP\)”](#))
- MCLR pin (see [Section 2.4 “Master Clear \(MCLR\) Pin”](#))
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see [Section 2.5 “ICSP Pins”](#))
- OSC1 and OSC2 pins when external oscillator source is used (see [Section 2.6 “External Oscillator Pins”](#))

2.2 Decoupling Capacitors

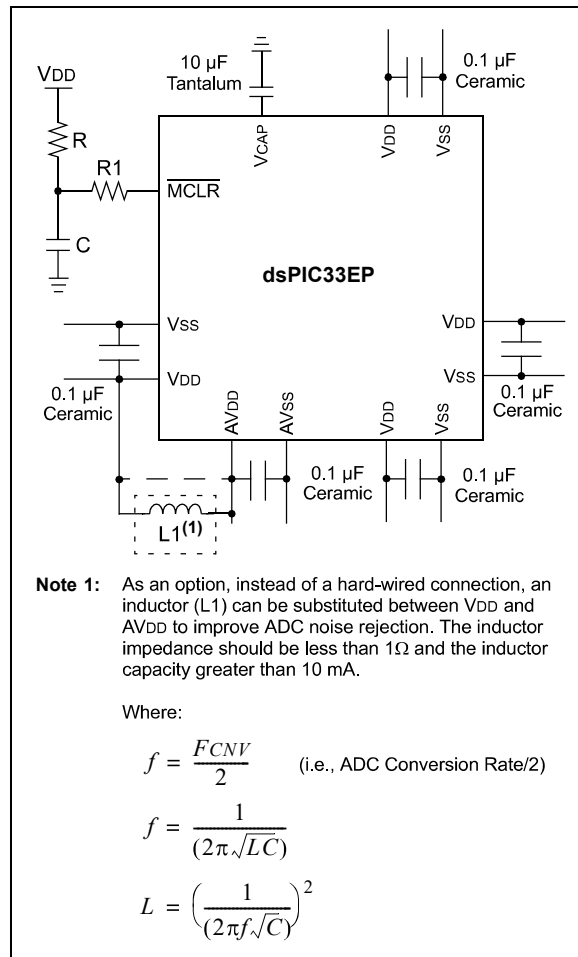
The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 μF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

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FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including DSCs, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See [Section 27.4 “On-Chip Voltage Regulator”](#) for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

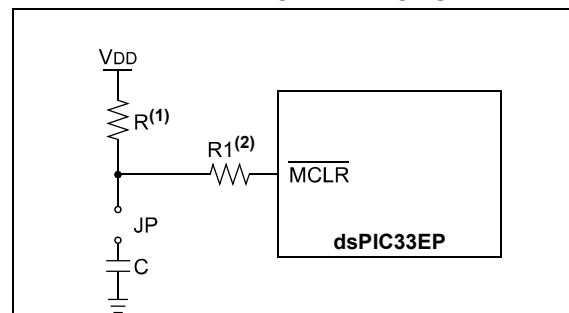
- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in [Figure 2-2](#), it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in [Figure 2-2](#), within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

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2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (VIH) and Voltage Input Low (VIL) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICKit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

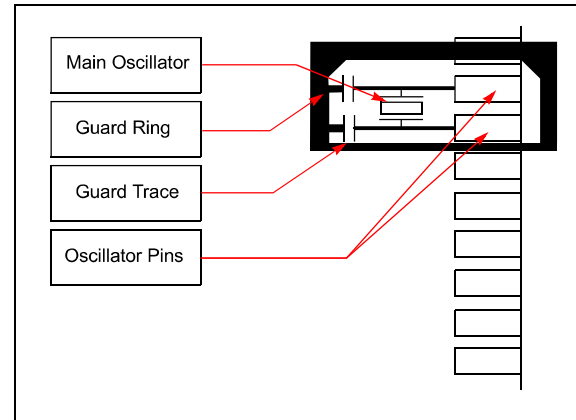
- “Using MPLAB® ICD 3 In-Circuit Debugger” (poster) (DS51765)
- “Development Tools Design Advisory” (DS51764)
- “MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide” (DS51616)
- “Using MPLAB® REAL ICE™ In-Circuit Emulator” (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see [Section 9.0 “Oscillator Configuration”](#) for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in [Figure 2-3](#).

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



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2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to $3 \text{ MHz} < F_{IN} < 5.5 \text{ MHz}$ to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings, after a POR with an oscillator frequency outside this range, will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

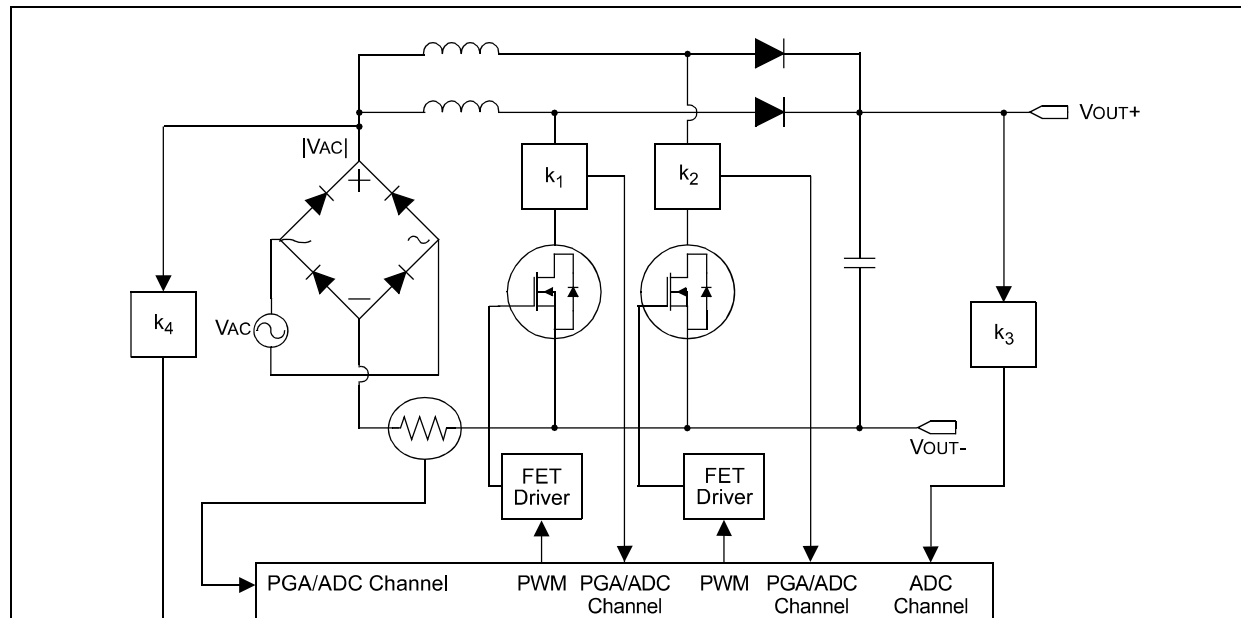
Alternatively, connect a 1k to 10k resistor between V_{SS} and unused pins, and drive the output to logic low.

2.9 Targeted Applications

- Power Factor Correction (PFC)
 - Interleaved PFC
 - Critical Conduction PFC
 - Bridgeless PFC
- DC/DC Converters
 - Buck, Boost, Forward, Flyback, Push-Pull
 - Half/Full-Bridge
 - Phase-Shift Full-Bridge
 - Resonant Converters
- DC/AC
 - Half/Full-Bridge Inverter
 - Resonant Inverter

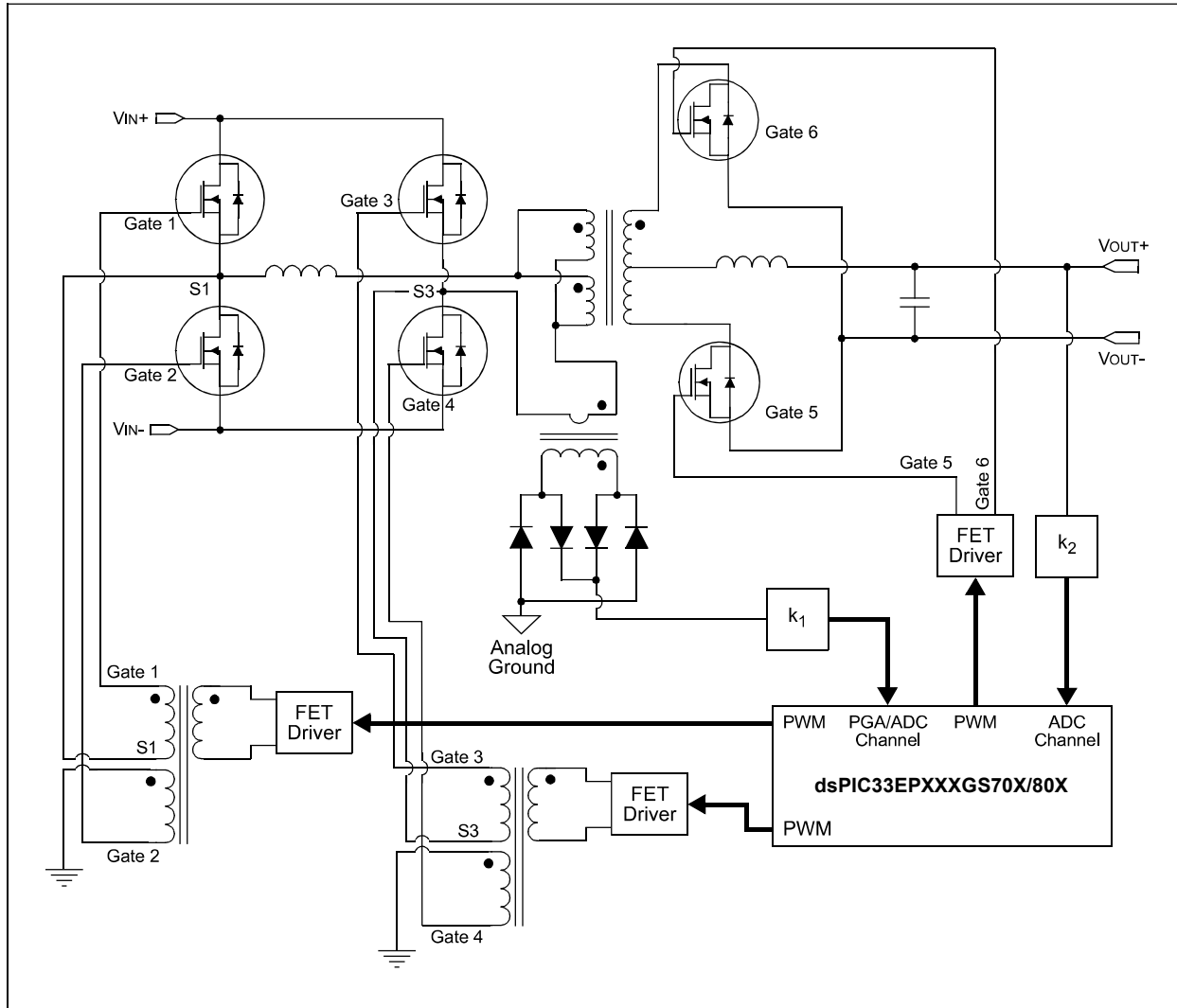
Examples of typical application connections are shown in [Figure 2-4](#) through [Figure 2-6](#).

FIGURE 2-4: INTERLEAVED PFC



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FIGURE 2-5: PHASE-SHIFTED FULL-BRIDGE CONVERTER



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FIGURE 2-6: OFF-LINE UPS

