Document Title

512Kx8 bit Low Voltage and Ultra Low Power CMOS Static RAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	May 1,2001	Preliminary
0B	1. Change for t_{PWE}: 45 to 40 ns for 55 ns product : 60 to 40 ns for 70 ns product 2. Change for V_{CC}: 2.2-3.6V to 2.7-3.6V 3.1 Change for I_{CC} test conditiomn: V_{CC}=Max. to 3V 3.2 Change for I_{CC}: 30 to 25mA for 55 ns product 25 to 20mA for 70 ns porduct 20 to 15 mA for 100 ns product 4.1 Change for V_{DR} Min. : 1.2 to 1.5V 4.2 Change for I_{DR} test condition: V_{CC}=1.2 to 1.5V and I_{DR} 5. Change for t_{HZCE} 25 to 20 ns for 55 ns product 6. Change for t_{HZWE} 33 to 30 ns for 70 ns product	August 31,2001	

512K x 8 LOW POWER and LOW Vcc CMOS STATIC RAM

FEATURES

- Access times of 55, 70, 100 ns
- CMOS Low power operation:
  - — 60 mW (typical) operation
  - — 3 µW (typical) standby
- Low data retention voltage: 1.5V (min.)
- Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) inputs for ease in applications
- TTL compatible inputs and outputs
- Fully static operation:
  - — No clock or refresh reguired
- Single 2.7V-3.6V power supply
- Available in the 32-pin 8*20mm TSOP-1, 32-pin 8*13.4mm TSOP-1 and 48-pin 6*8mm TF-BGA

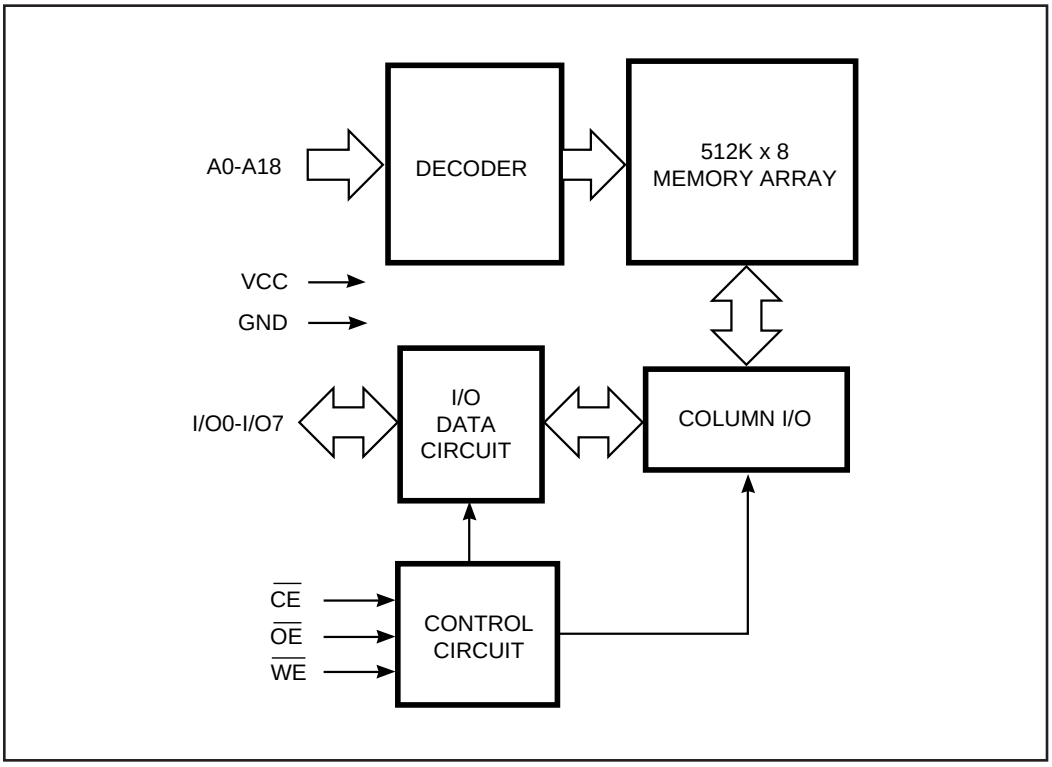
DESCRIPTION

The *ICSI* IC62LV5128L and IC62LV5128LL is a low voltage, 524,288 words by 8 bits, CMOS SRAM. It is fabricated using *ICSI*'s low voltage, six transistor (6T), CMOS technology. The device is targeted to satisfy the demands of the state-of-the-art technologies such as cell phones and pagers.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Additionally, easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

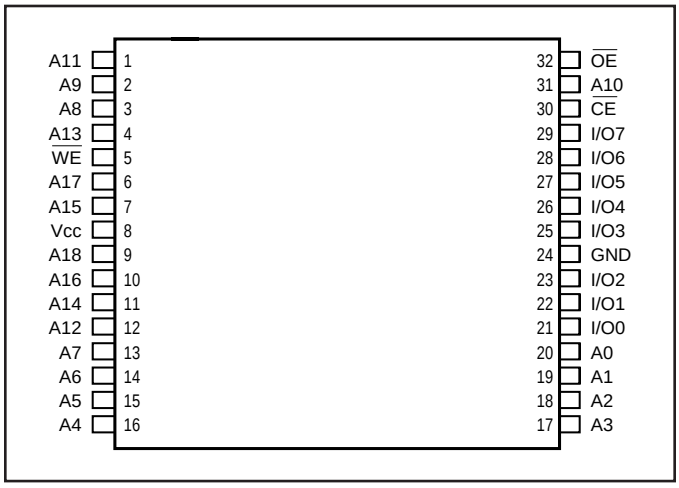
The IC62LV5128L and IC62LV5128LL are available in 32-pin 8*20mm TSOP-1, 8*13.4mm TSOP-1 and 48-pin 6*8mm TF-BGA.

FUNCTIONAL BLOCK DIAGRAM

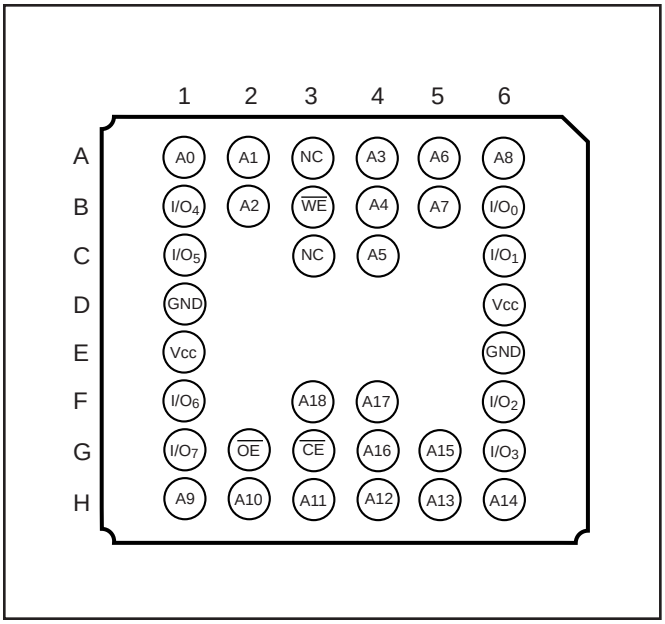


PIN CONFIGURATIONS

32-Pin 8*20mm TSOP-1, 8*13.4mm STSOP-1



48-Pin 6*8mm TF-BGA



PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Data Input/Output
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V - 3.6V
Industrial	–40°C to +85°C	2.7V - 3.6V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
V_{CC}	Vcc related to GND	–0.3 to +4.0	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1][2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.0 V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage[1]		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]		–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	–1	1	µA

Notes:
1. V_{IH}(max) =V_{CC} +2.0V for pulse width less than 10ns.
2. V_{IL}(min) = –2.0V for pulse width less than 10 ns.

IC62LV5128L POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = 3V, $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	25 25	— —	20 20	— —	15 15	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}	Com. Ind.	— —	0.2 0.3	— —	0.2 0.3	— —	0.2 0.3	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0 $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	Com. Ind.	— —	35 50	— —	35 50	— —	35 50	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IC62LV5128LL POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = 3V, $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	25 25	— —	20 20	— —	15 15	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}	Com. Ind.	— —	0.2 0.3	— —	0.2 0.3	— —	0.3 0.3	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0 $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	Com. Ind.	— —	15 20	— —	15 20	— —	15 20	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	100	ns
t_{OHA}	Output Hold Time	10	—	10	—	15	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	55	—	70	—	100	ns
t_{DOE}	$\overline{OE}$ Access Time	—	30	—	35	—	50	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	0	25	0	30	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	10	—	10	—	10	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	20	0	25	0	30	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input Reference Level	1.3V
Output Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

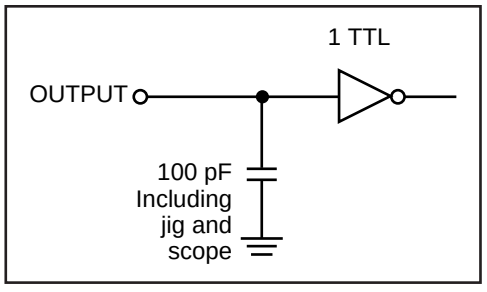


Figure 1

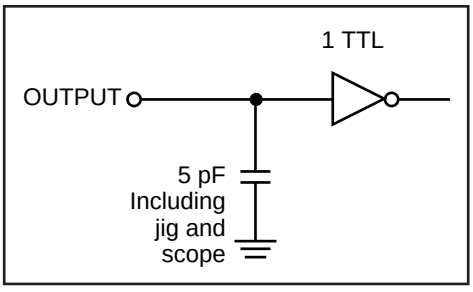
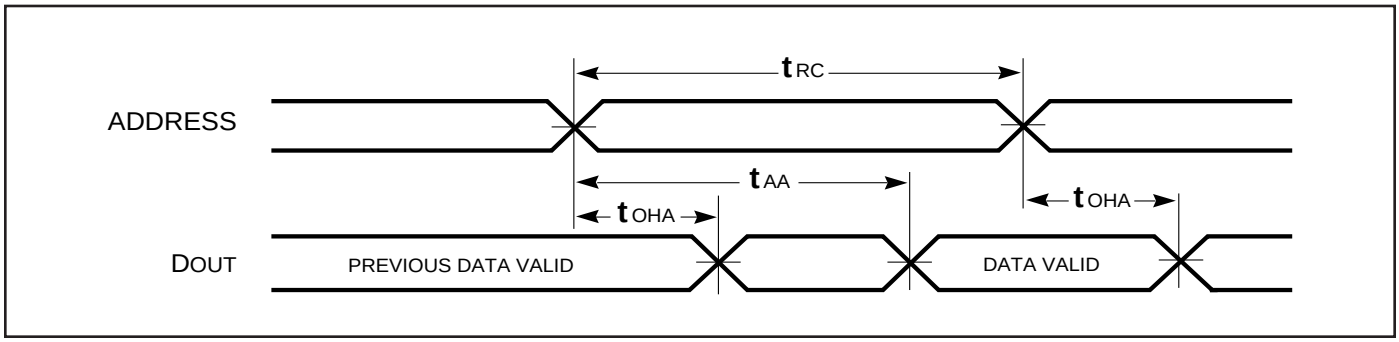
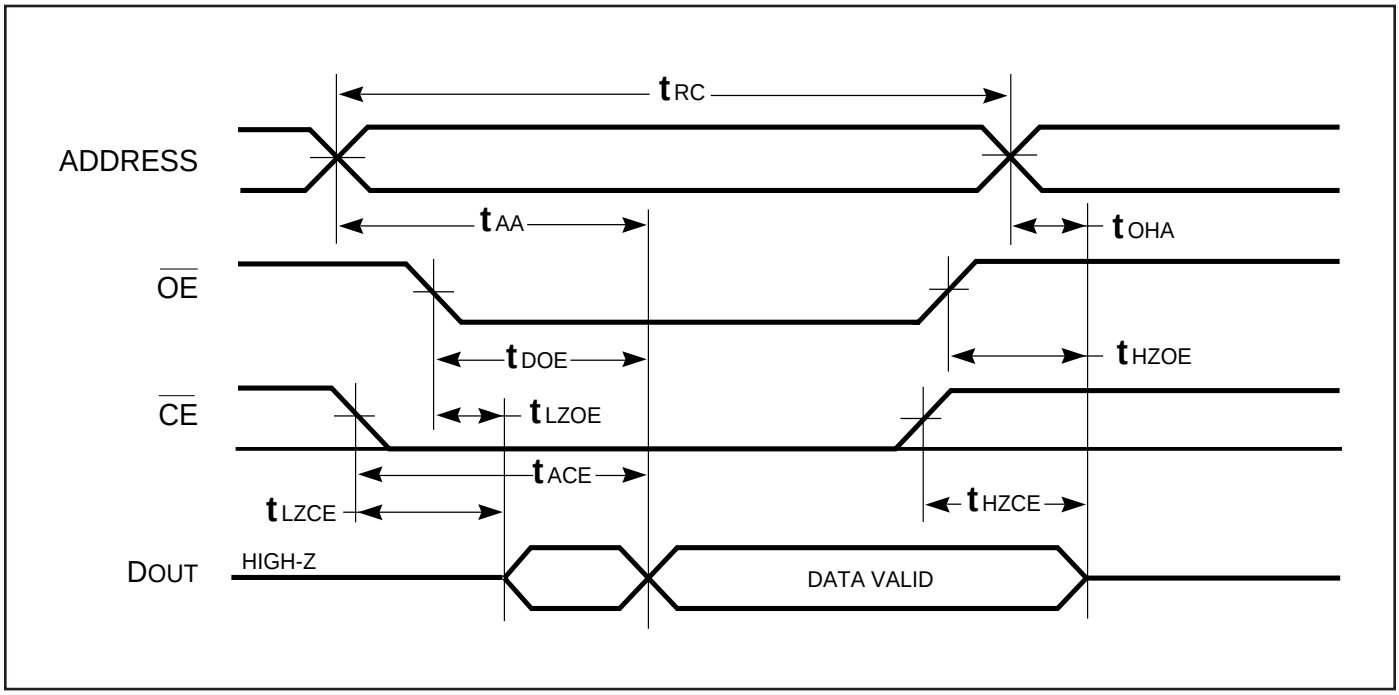


Figure 2

AC TEST LOADS
READ CYCLE NO.1[1,2]



AC WAVEFORMS
READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

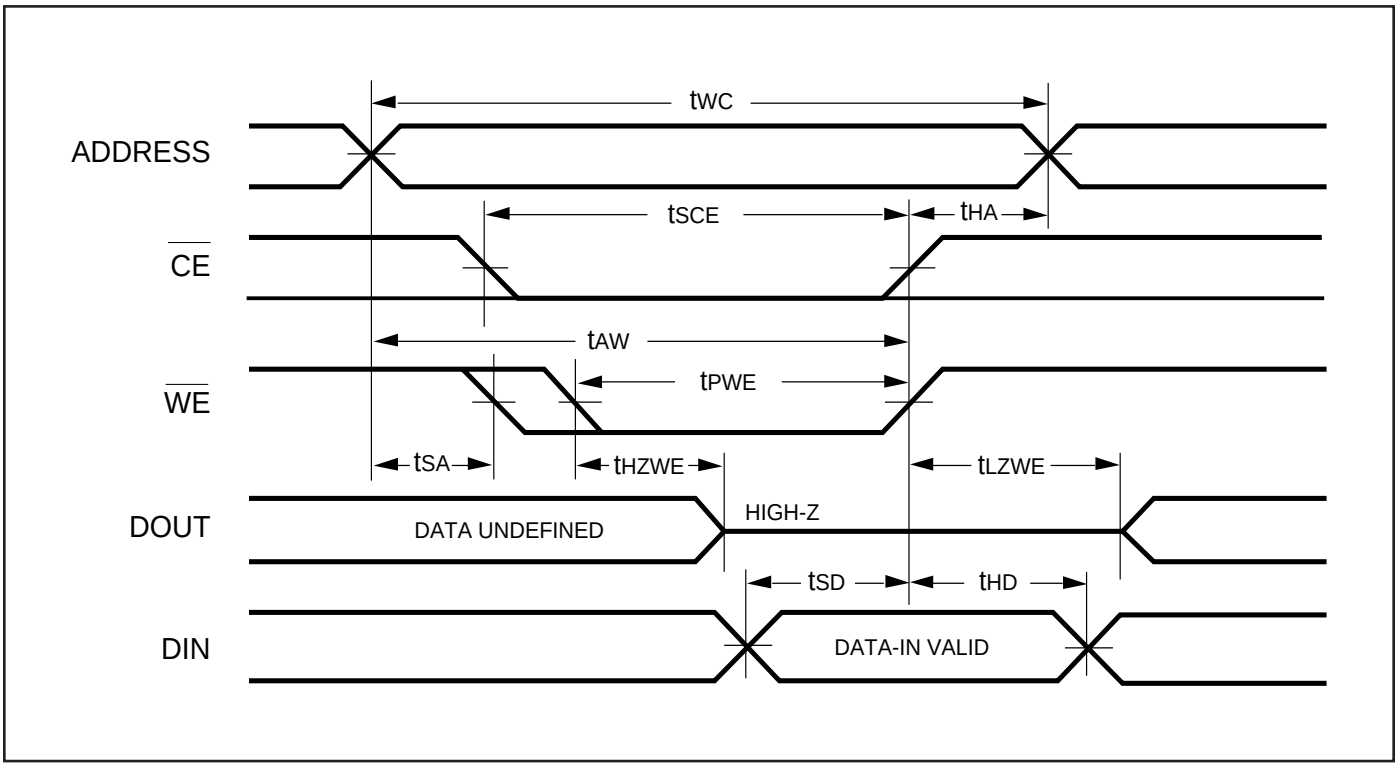
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range, Standard and Low Power)

		-55		-70		-100		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max	Unit
t_{WC}	Write Cycle Time	55	—	70	—	100	—	ns
t_{SCE}	$\overline{CE}$ to Write End	50	—	65	—	80	—	ns
t_{AW}	Address Setup Time to Write End	50	—	65	—	80	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	40	—	40	—	80	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	40	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	30	—	30	—	40	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

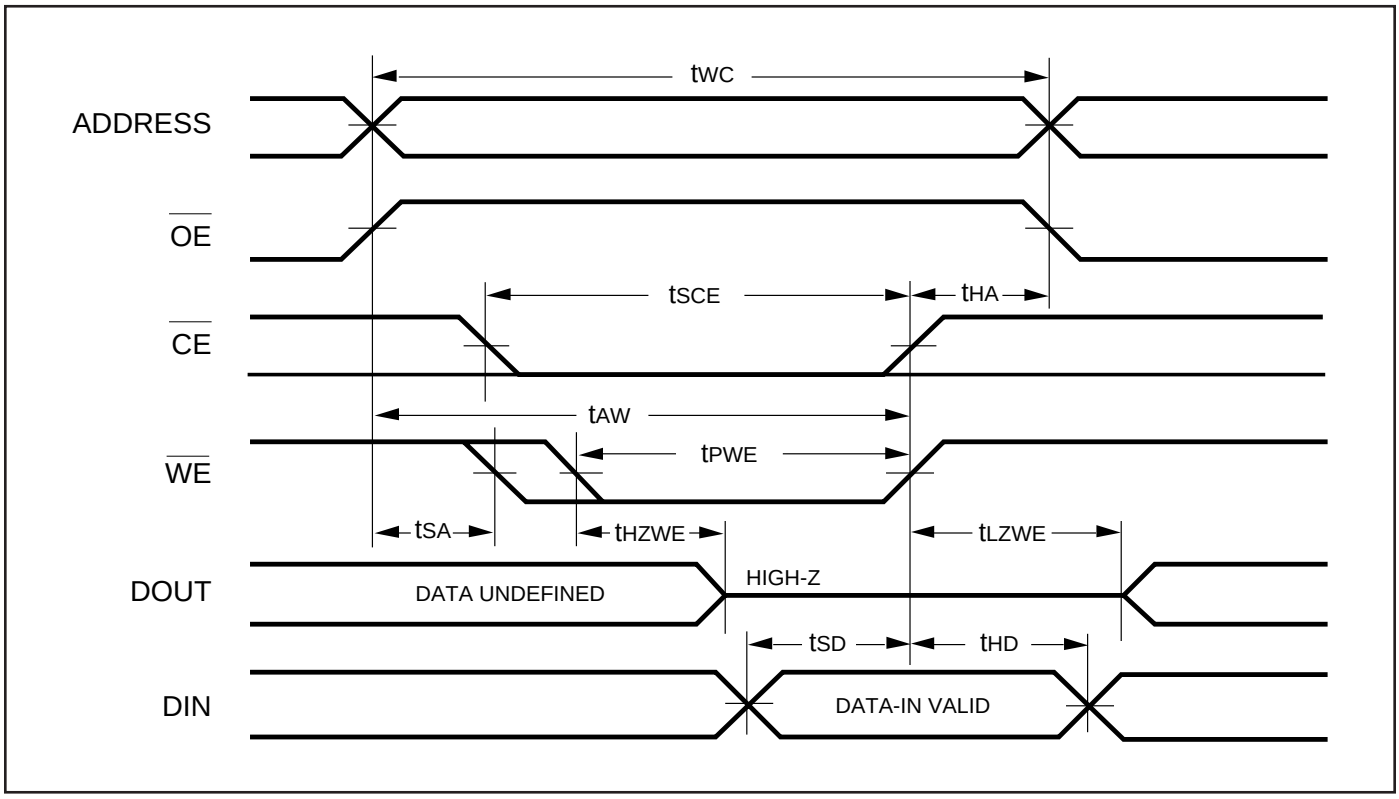
Notes:
1. Test conditions assume signal transition times of 5 ns or less, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

AC WAVEFORMS

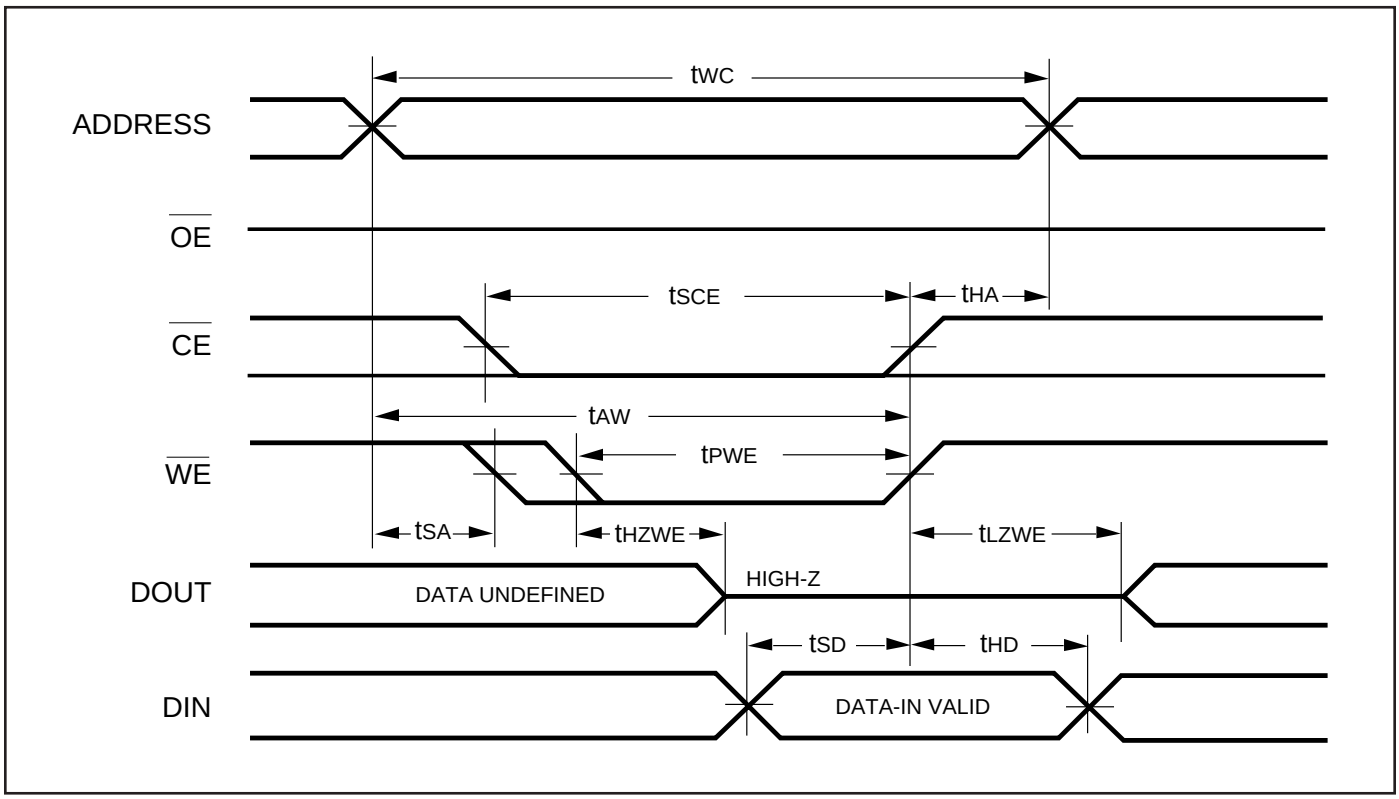
WRITE CYCLE NO. 1 ($\overline{CE}$ Controlled)



WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)[1]



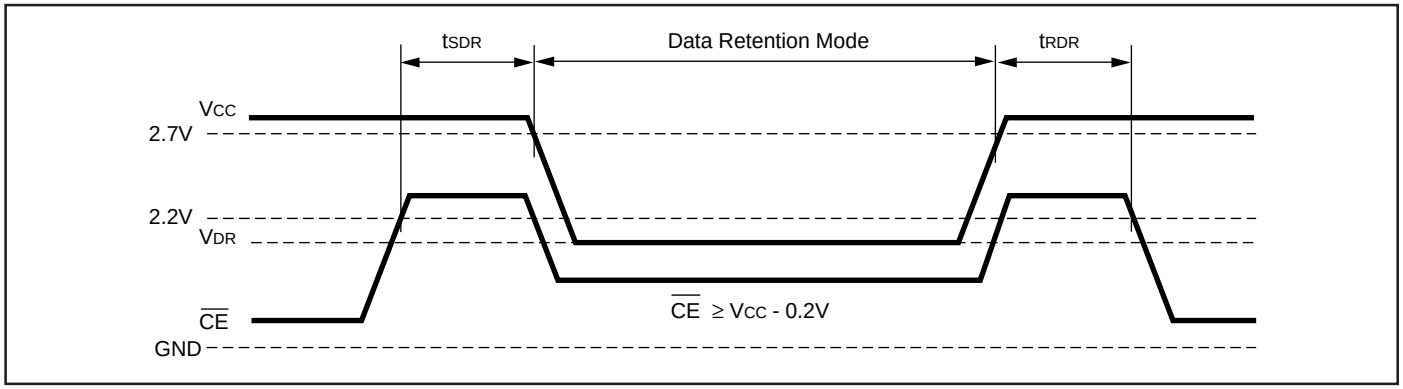
WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)[1]



DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform		1.5	3.6	V
I_{DR}	Data Retention Current	Vcc = 1.5V, $\overline{CE} \geq$ Vcc – 0.2V	Com. (-L)	—	10	µA
			Com. (-LL)	—	5	µA
			Ind. (-L)	—	15	µA
			Ind. (-LL)	—	9	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		5	—	ns

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IC62LV5128L-55T	8*20mm TSOP-1
	IC62LV5128L-55H	8*13.4mm TSOP-1
	IC62LV5128L-55B	6*8mm TF-BGA
70	IC62LV5128L-70T	8*20mm TSOP-1
	IC62LV5128L-70H	8*13.4mm TSOP-1
	IC62LV5128L-70B	6*8mm TF-BGA
100	IC62LV5128L-100T	8*20mm TSOP-1
	IC62LV5128L-100H	8*13.4mm TSOP-1
	IC62LV5128L-100B	6*8mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IC62LV5128L-55TI	8*20mm TSOP-1
	IC62LV5128L-55HI	8*13.4mm TSOP-1
	IC62LV5128L-55BI	6*8mm TF-BGA
70	IC62LV5128L-70TI	8*20mm TSOP-1
	IC62LV5128L-70HI	8*13.4mm TSOP-1
	IC62LV5128L-70BI	6*8mm TF-BGA
100	IC62LV5128L-100TI	8*20mm TSOP-1
	IC62LV5128L-100HI	8*13.4mm TSOP-1
	IC62LV5128L-100BI	6*8mm TF-BGA

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IC62LV5128LL-55T	8*20mm TSOP-1
	IC62LV5128LL-55H	8*13.4mm TSOP-1
	IC62LV5128LL-55B	6*8mm TF-BGA
70	IC62LV5128LL-70T	8*20mm TSOP-1
	IC62LV5128LL-70H	8*13.4mm TSOP-1
	IC62LV5128LL-70B	6*8mm TF-BGA
100	IC62LV5128LL-100T	8*20mm TSOP-1
	IC62LV5128LL-100H	8*13.4mm TSOP-1
	IC62LV5128LL-100B	6*8mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IC62LV5128LL-55TI	8*20mm TSOP-1
	IC62LV5128LL-55HI	8*13.4mm TSOP-1
	IC62LV5128LL-55BI	6*8mm TF-BGA
70	IC62LV5128LL-70TI	8*20mm TSOP-1
	IC62LV5128LL-70HI	8*13.4mm TSOP-1
	IC62LV5128LL-70BI	6*8mm TF-BGA
100	IC62LV5128LL-100TI	8*20mm TSOP-1
	IC62LV5128LL-100HI	8*13.4mm TSOP-1
	IC62LV5128LL-100BI	6*8mm TF-BGA

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