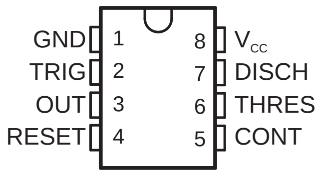
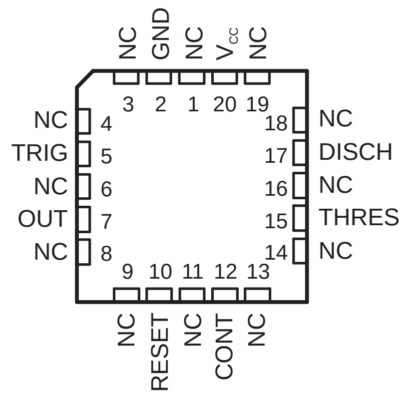
FEATURES

- **Timing From Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source up to 200 mA**

NA555...D OR P PACKAGE
NE555...D, P, PS, OR PW PACKAGE
SA555...D OR P PACKAGE
SE555...D, JG, OR P PACKAGE
(TOP VIEW)



SE555...FK PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

ORDERING INFORMATION(1)

T_A	V_{THRES} MAX V_{CC} = 15 V	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	11.2 V	PDIP – P	Tube of 50	NE555P	NE555P
		SOIC – D	Tube of 75	NE555D	NE555
			Reel of 2500	NE555DR	
		SOP – PS	Reel of 2000	NE555PSR	N555
		TSSOP – PW	Tube of 150	NE555PW	N555
			Reel of 2000	NE555PWR	
–40°C to 85°C	11.2 V	PDIP – P	Tube of 50	SA555P	SA555P
		SOIC – D	Tube of 75	SA555D	SA555
			Reel of 2000	SA555DR	
–40°C to 105°C	11.2 V	PDIP – P	Tube of 50	NA555P	NA555P
		SOIC – D	Tube of 75	NA555D	NA555
			Reel of 2000	NA555DR	
–55°C to 125°C	10.6	PDIP – P	Tube of 50	SE555P	SE555P
		SOIC – D	Tube of 75	SE555D	SE555D
			Reel of 2500	SE555DR	
		CDIP – JG	Tube of 50	SE555JG	SE555JG
		LCCC – FK	Tube of 55	SE555FK	SE555FK

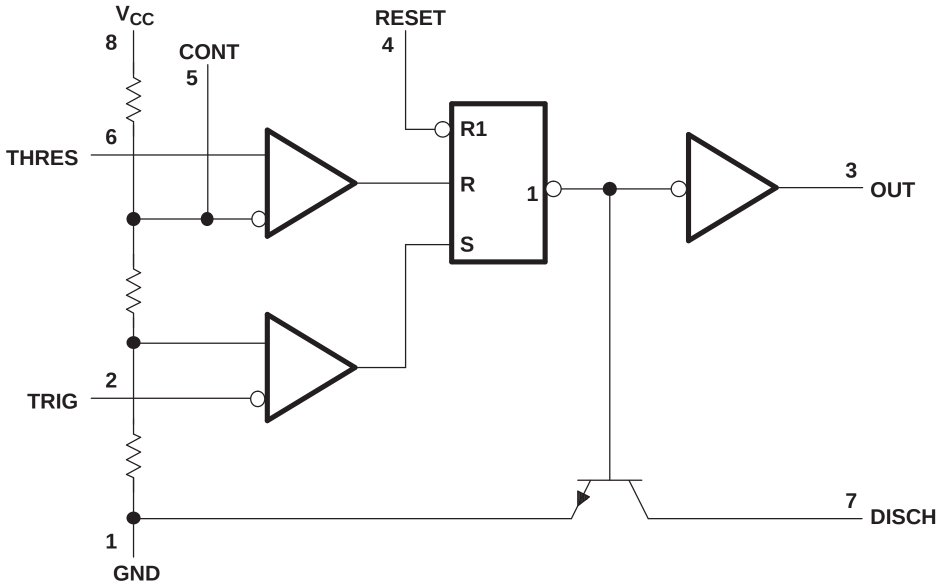
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

RESET	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{CC}	Irrelevant	High	Off
High	>1/3 V_{CC}	>2/3 V_{CC}	Low	On
High	>1/3 V_{CC}	<2/3 V_{CC}	As previously established	

(1) Voltage levels shown are nominal.

FUNCTIONAL BLOCK DIAGRAM



A. Pin numbers shown are for the D, JG, P, PS, and PW packages.

B. RESET can override TRIG, which can override THRES.

TEXAS INSTRUMENTS
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Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]			18	V
V_I	Input voltage	CONT, RESET, THRES, TRIG		V_{CC}	V
I_O	Output current			±225	mA
θ_{JA}	Package thermal impedance[3][4]	D package		97	°C/W
		P package		85	
		PS package		95	
		PW package		149	
θ_{JC}	Package thermal impedance[5][6]	FK package		5.61	°C/W
		JG package		14.5	
T_J	Operating virtual junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1, 6 mm (1/16 in) from case for 60 s	JG package		300	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA.}$ Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) Maximum power dissipation is a function of T_J(max), θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with MIL-STD-883.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	NA555, NE555, SA555	4.5	16	V
		SE555	4.5	18	
V_I	Input voltage	CONT, RESET, THRES, and TRIG		V_{CC}	V
I_O	Output current			±200	mA
T_A	Operating free-air temperature	NA555	–40	105	°C
		NE555	0	70	
		SA555	–40	85	
		SE555	–55	125	

Electrical Characteristics

V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555 MIN	SE555 TYP	SE555 MAX	NA555, NE555, SA555 MIN	NA555, NE555, SA555 TYP	NA555, NE555, SA555 MAX	UNIT
THRES voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
THRES current(1)				30	250		30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
		T_A = –55°C to 125°C	3		6				
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
		T_A = –55°C to 125°C			1.9				
TRIG current	TRIG at 0 V			0.5	0.9		0.5	2	μA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	T_A = –55°C to 125°C				1.1				
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0 V			–0.4	–1		–0.4	–1.5	
DISCH switch off-state current				20	100		20	100	nA
CONT voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
		T_A = –55°C to 125°C	9.6		10.4				
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
		T_A = –55°C to 125°C	2.9		3.8				
Low-level output voltage	V_{CC} = 15 V, I_{OL} = 10 mA			0.1	0.15		0.1	0.25	V
		T_A = –55°C to 125°C			0.2				
	V_{CC} = 15 V, I_{OL} = 50 mA			0.4	0.5		0.4	0.75	
		T_A = –55°C to 125°C			1				
	V_{CC} = 15 V, I_{OL} = 100 mA			2	2.2		2	2.5	
		T_A = –55°C to 125°C			2.7				
	V_{CC} = 15 V, I_{OL} = 200 mA			2.5			2.5		
	V_{CC} = 5 V, I_{OL} = 3.5 mA	T_A = –55°C to 125°C			0.35				
	V_{CC} = 5 V, I_{OL} = 5 mA			0.1	0.2		0.1	0.35	
		T_A = –55°C to 125°C			0.8				
	V_{CC} = 5 V, I_{OL} = 8 mA			0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V, I_{OL} = –100 mA		13	13.3		12.75	13.3		V
		T_A = –55°C to 125°C	12						
	V_{CC} = 15 V, I_{OH} = –200 mA			12.5			12.5		
	V_{CC} = 15 V, I_{OL} = –100 mA		3	3.3		2.75	3.3		
		T_A = –55°C to 125°C	2						
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

(1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \approx 3.4$ MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

TEXAS INSTRUMENTS
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Operating Characteristics

V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval(2)	Each timer, monostable(3)	T_A = 25°C		0.5	1.5(4)		1	3	%
	Each timer, astable(5)			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable(3)	T_A = MIN to MAX		30	100(4)		50		ppm/°C
	Each timer, astable(5)			90			150		
Supply-voltage sensitivity of timing interval	Each timer, monostable(3)	T_A = 25°C		0.05	0.2(4)		0.1	0.5	%/V
	Each timer, astable(5)			0.15			0.3		
Output-pulse rise time		C_L = 15 pF, T_A = 25°C		100	200(4)		100	300	ns
Output-pulse fall time		C_L = 15 pF, T_A = 25°C		100	200(4)		100	300	ns

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
(3) Values specified are for a device in a monostable circuit similar to Figure 9, with the following component values: R_A = 2 kΩ to 100 kΩ, C = 0.1 µF.
(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(5) Values specified are for a device in an astable circuit similar to Figure 12, with the following component values: R_A = 1 kΩ to 100 kΩ, C = 0.1 µF.

TYPICAL CHARACTERISTICS

Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

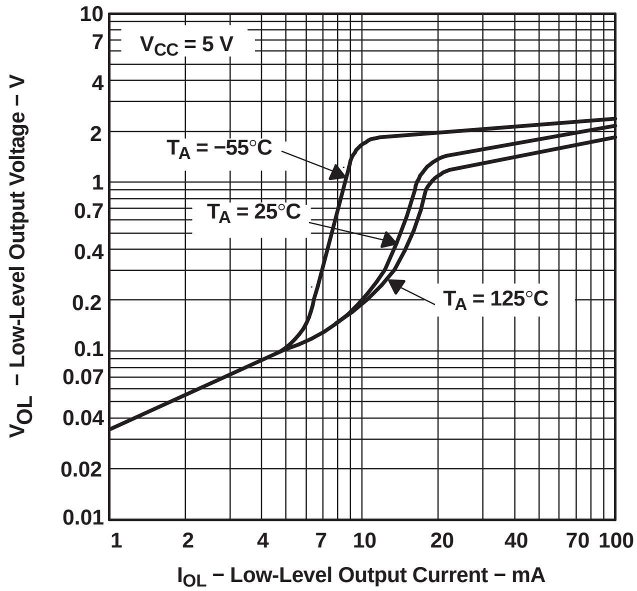


Figure 1.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

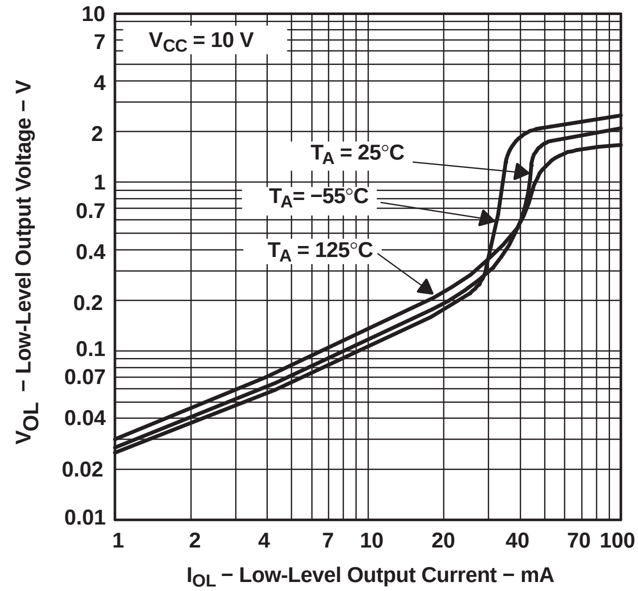


Figure 2.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

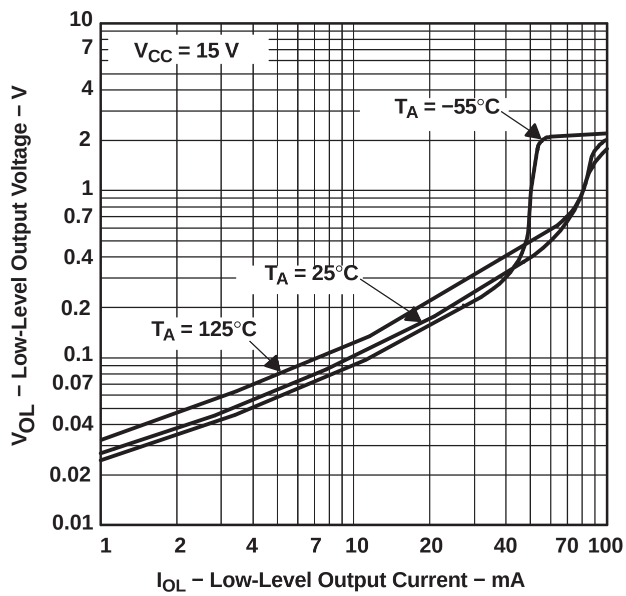


Figure 3.

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT

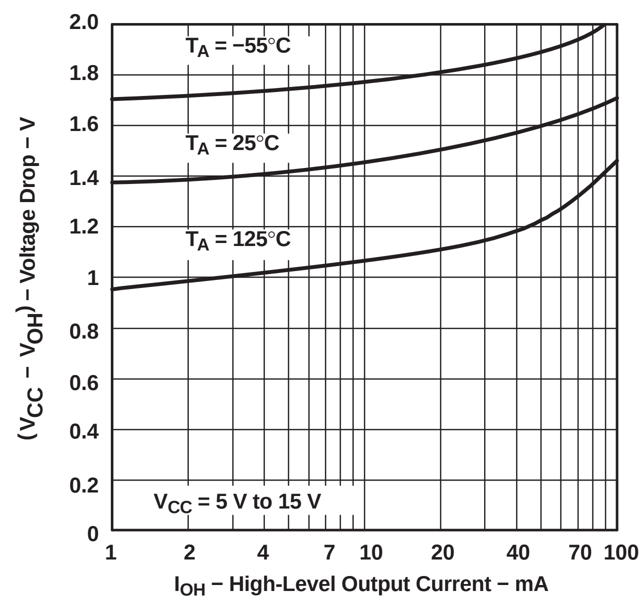


Figure 4.

TYPICAL CHARACTERISTICS (continued)

Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

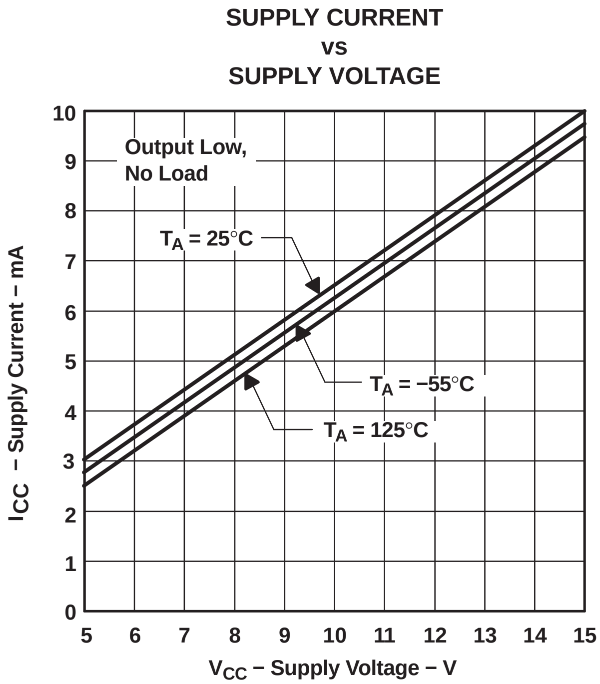


Figure 5.

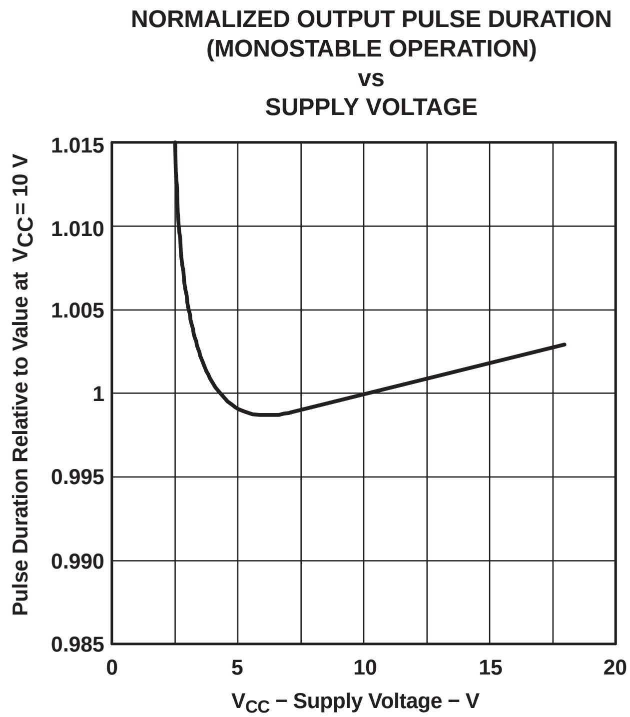


Figure 6.

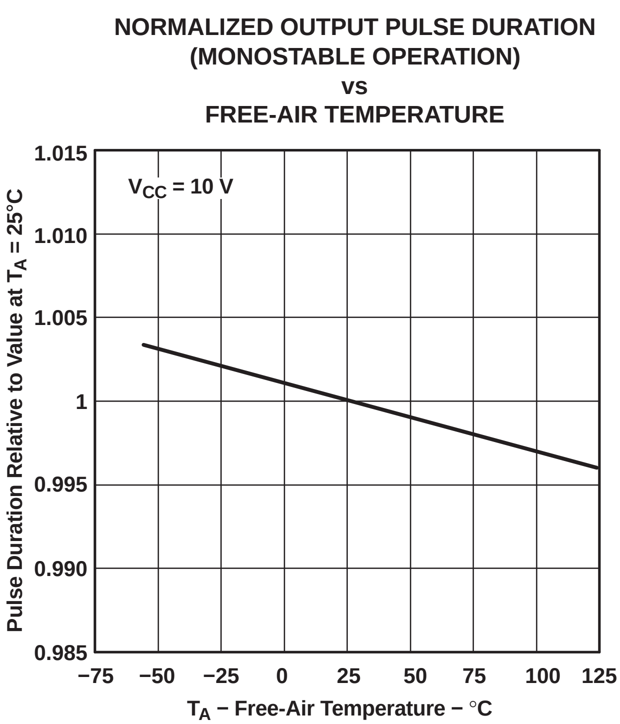


Figure 7.

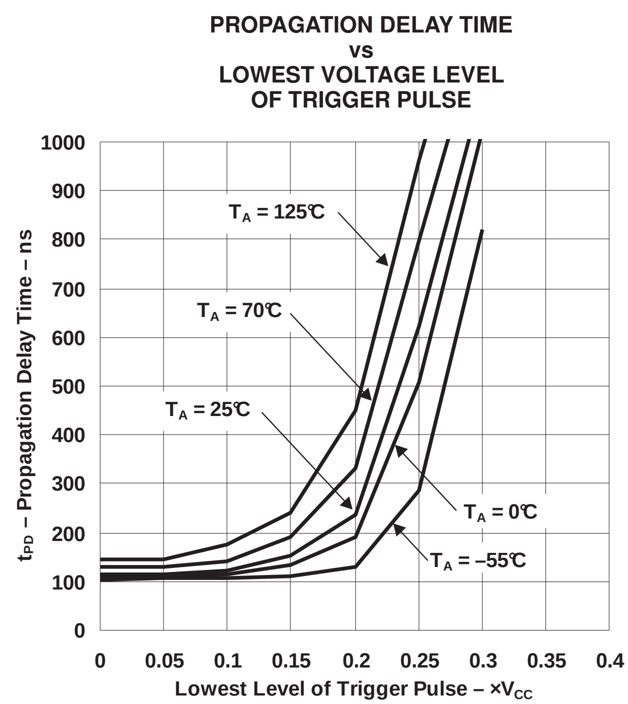
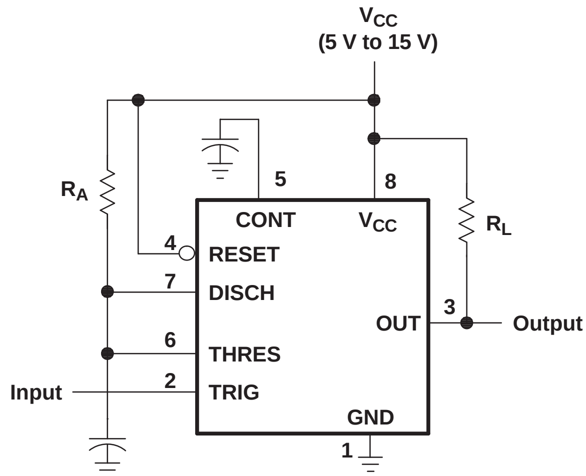


Figure 8.

APPLICATION INFORMATION

Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

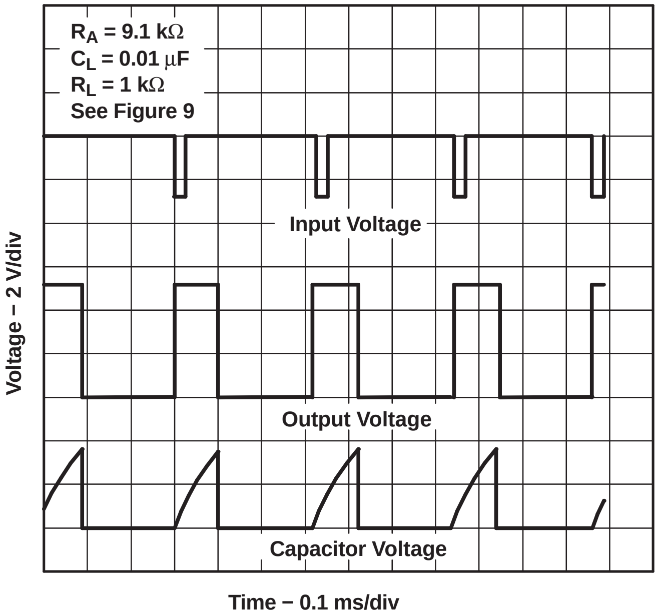


Figure 10. Typical Monostable Waveforms

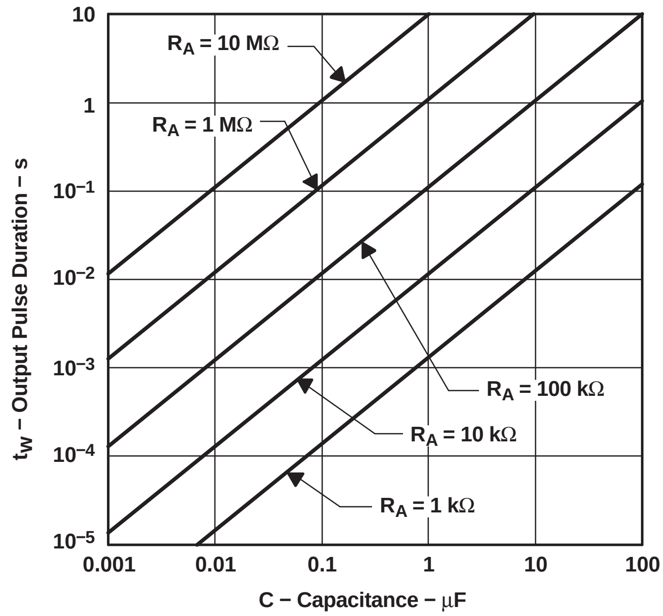
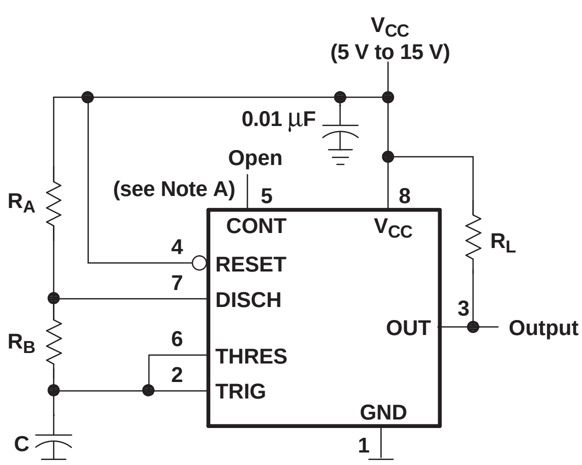


Figure 11. Output Pulse Duration vs Capacitance

Astable Operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

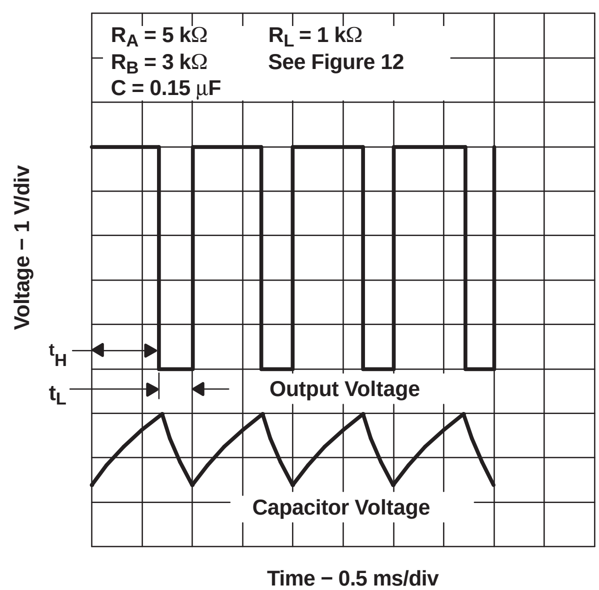


Figure 13. Typical Astable Waveforms

Figure 12 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693\,(R_A + R_B)\,C$$

$$t_L = 0.693\,(R_B)\,C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\,(R_A + 2R_B)\,C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\,C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

Output waveform duty cycle

$$= \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

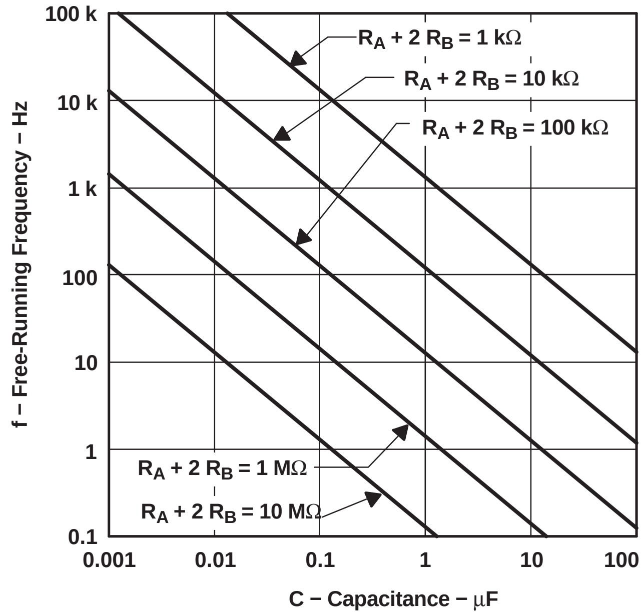
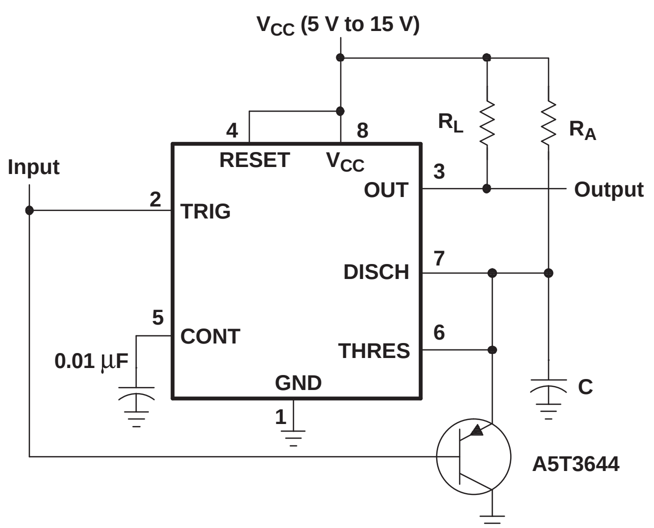


Figure 14. Free-Running Frequency

Missing-Pulse Detector

The circuit shown in Figure 15 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 16.



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 15. Circuit for Missing-Pulse Detector

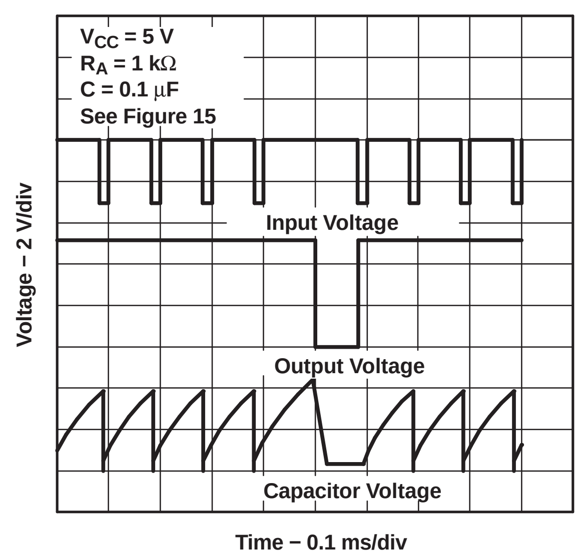


Figure 16. Completed Timing Waveforms for Missing-Pulse Detector

Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

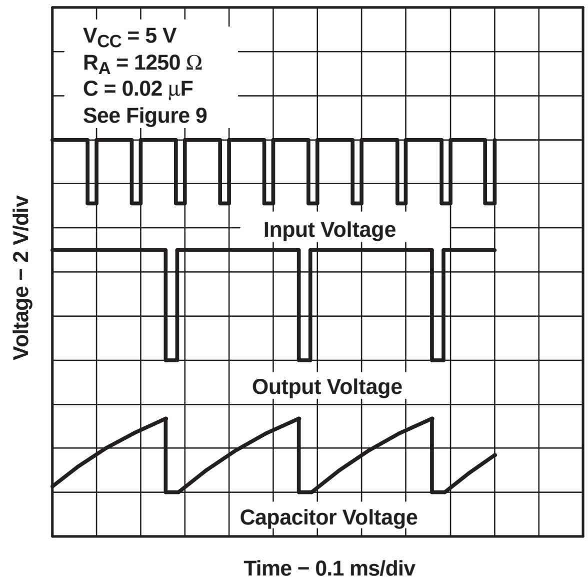
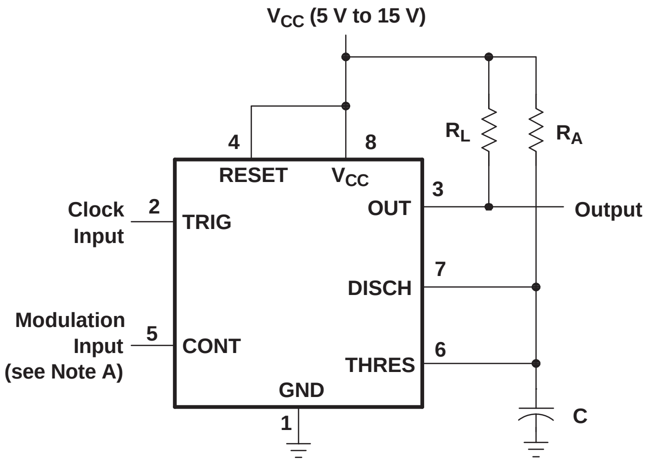


Figure 17. Divide-by-Three Circuit Waveforms

Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

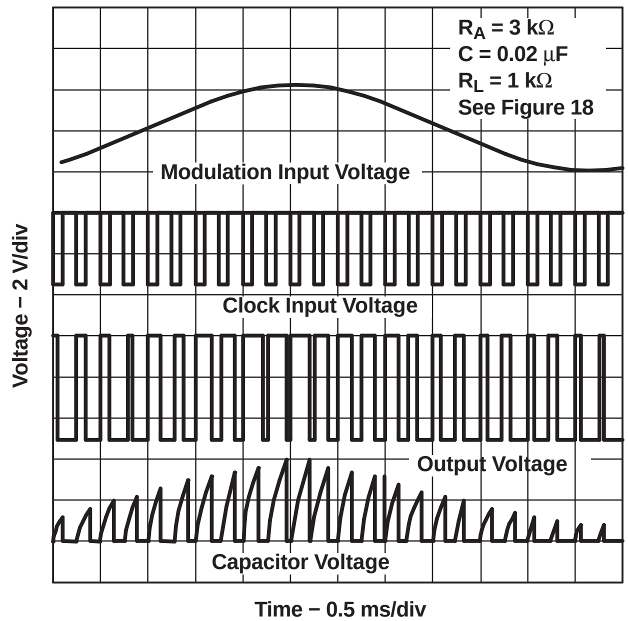
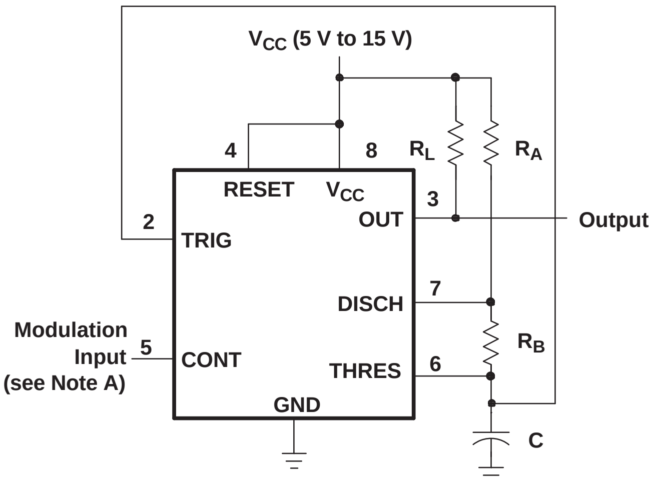


Figure 19. Pulse-Width-Modulation Waveforms

Pulse-Position Modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

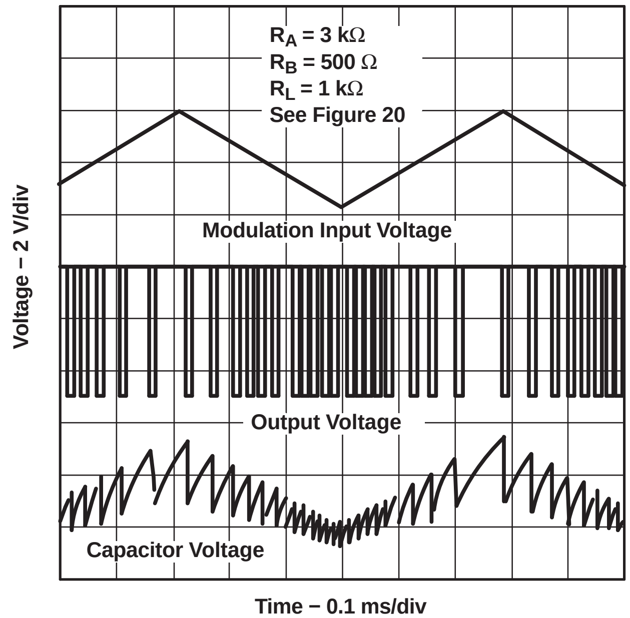
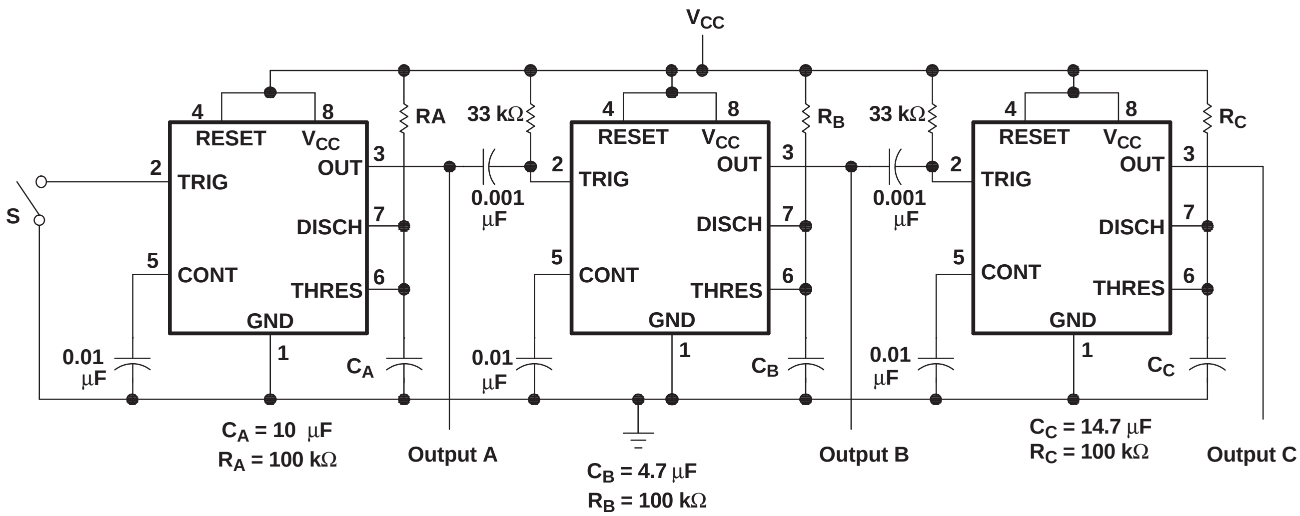


Figure 21. Pulse-Position-Modulation Waveforms

Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: S closes momentarily at t = 0.

Figure 22. Sequential Timer Circuit

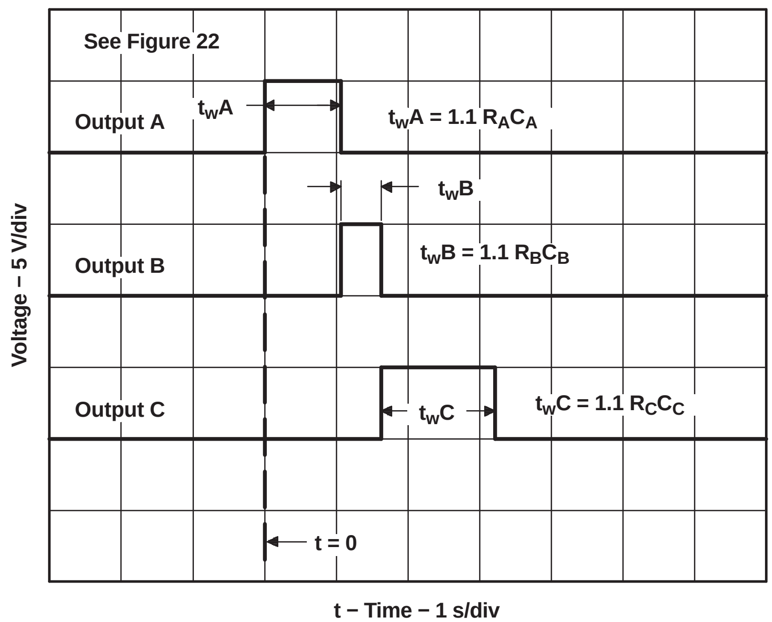


Figure 23. Sequential Timer Waveforms

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
JM38510/10901BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
NA555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NA555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NA555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DRG3	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI
NE555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
NE555PSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI
NE555PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
NE555Y	OBSOLETE			0		TBD	Call TI	Call TI
SA555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SA555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SE555D	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
SE555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SE555DR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
SE555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SE555FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SE555JG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
SE555JGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
SE555N	OBSOLETE	PDIP	N	8		TBD	Call TI	Call TI
SE555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SE555, SE555M :

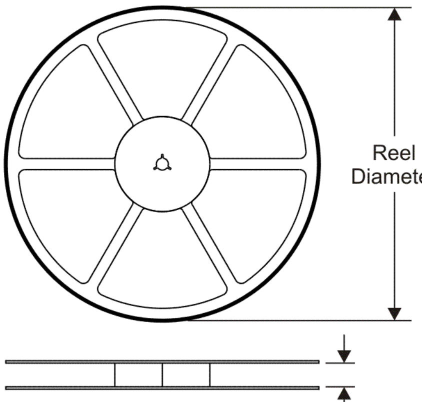
- Space: SE555-SP

NOTE: Qualified Version Definitions:

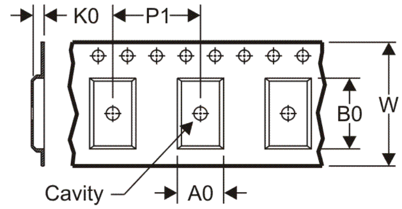
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

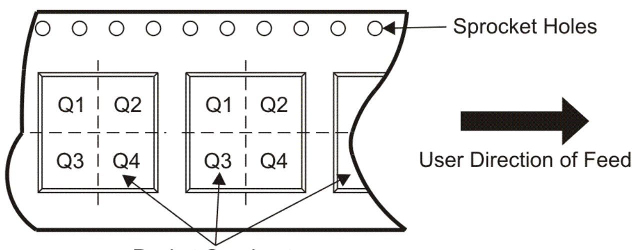


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

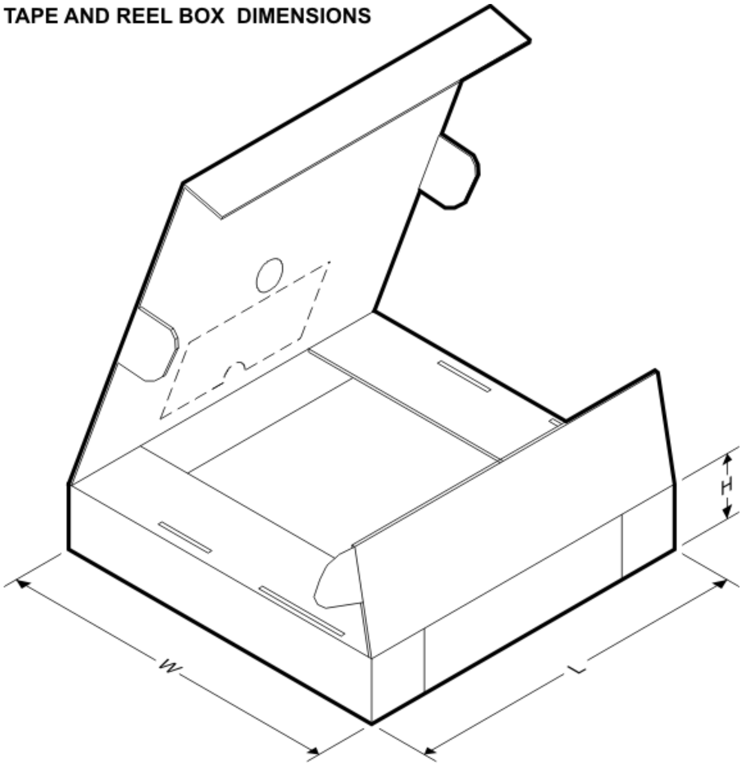
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
NE555PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

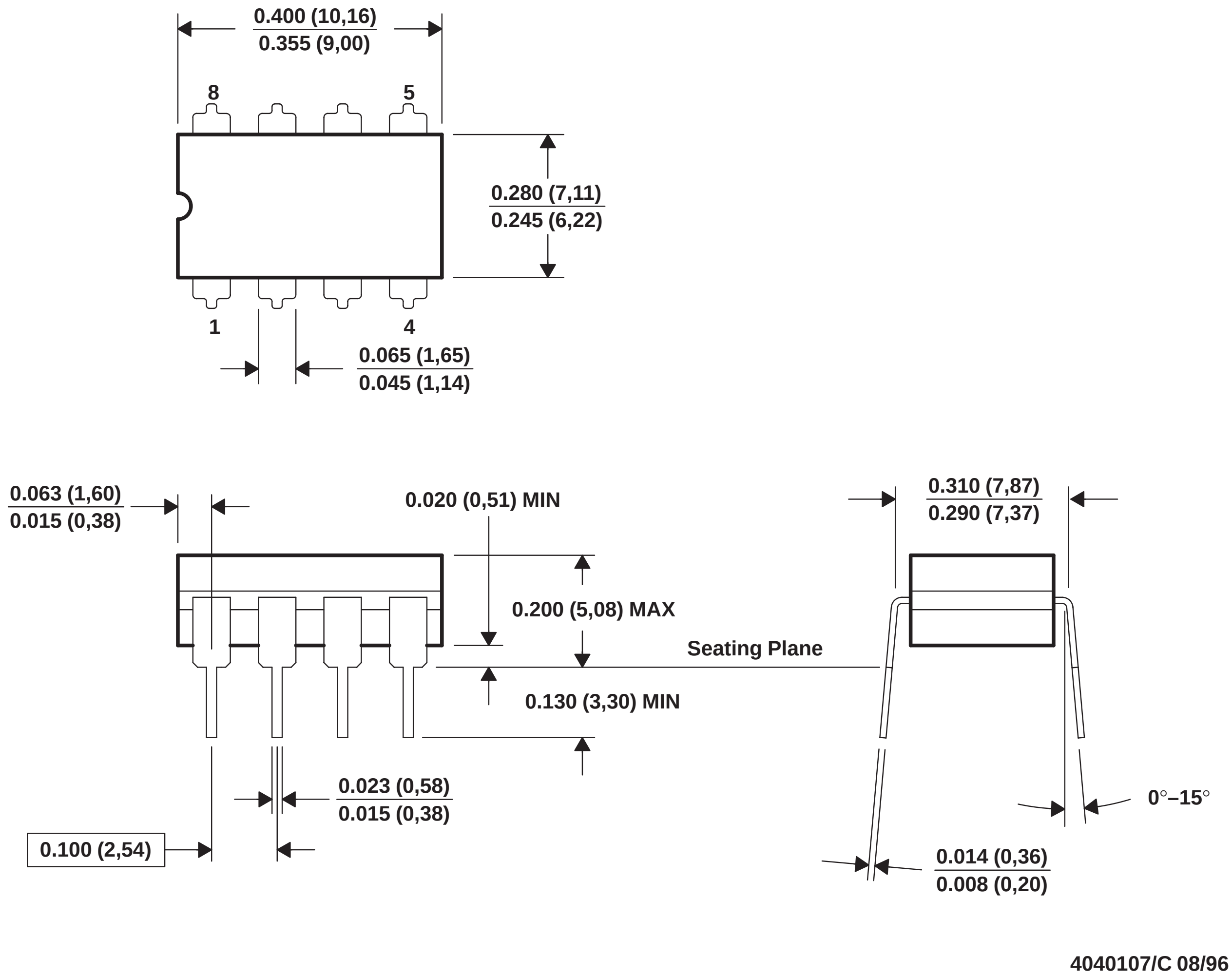
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NA555DR	SOIC	D	8	2500	340.5	338.1	20.6
NA555DR	SOIC	D	8	2500	346.0	346.0	29.0
NE555DR	SOIC	D	8	2500	346.0	346.0	29.0
NE555DR	SOIC	D	8	2500	340.5	338.1	20.6
NE555PSR	SO	PS	8	2000	346.0	346.0	33.0
NE555PWR	TSSOP	PW	8	2000	346.0	346.0	29.0
SA555DR	SOIC	D	8	2500	340.5	338.1	20.6

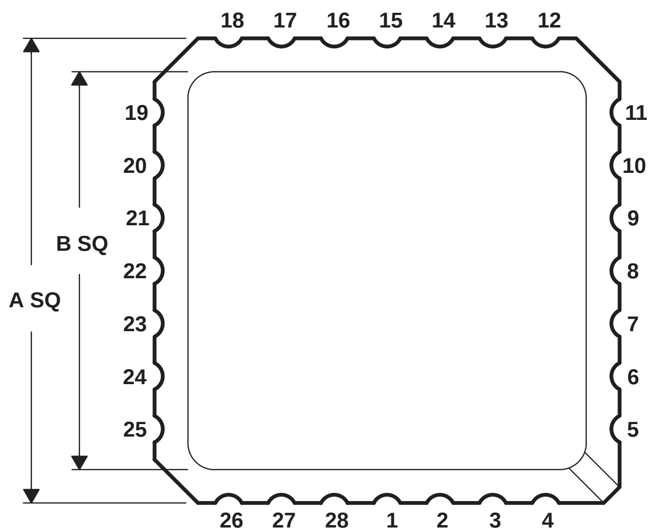
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



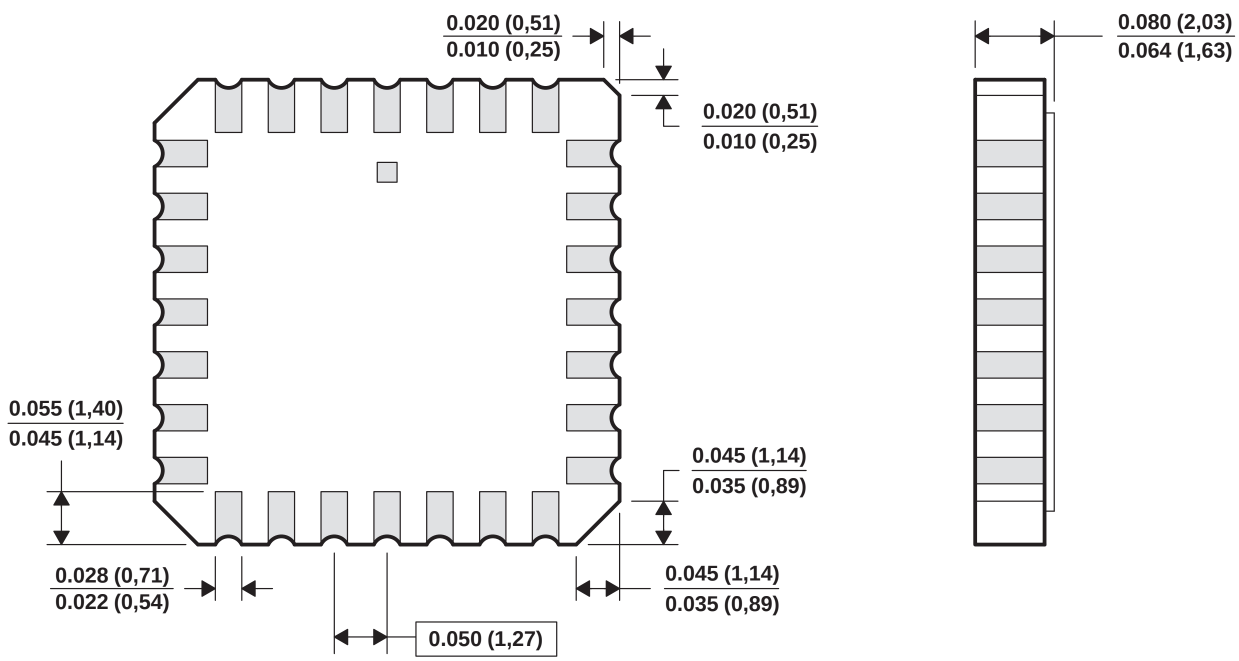
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



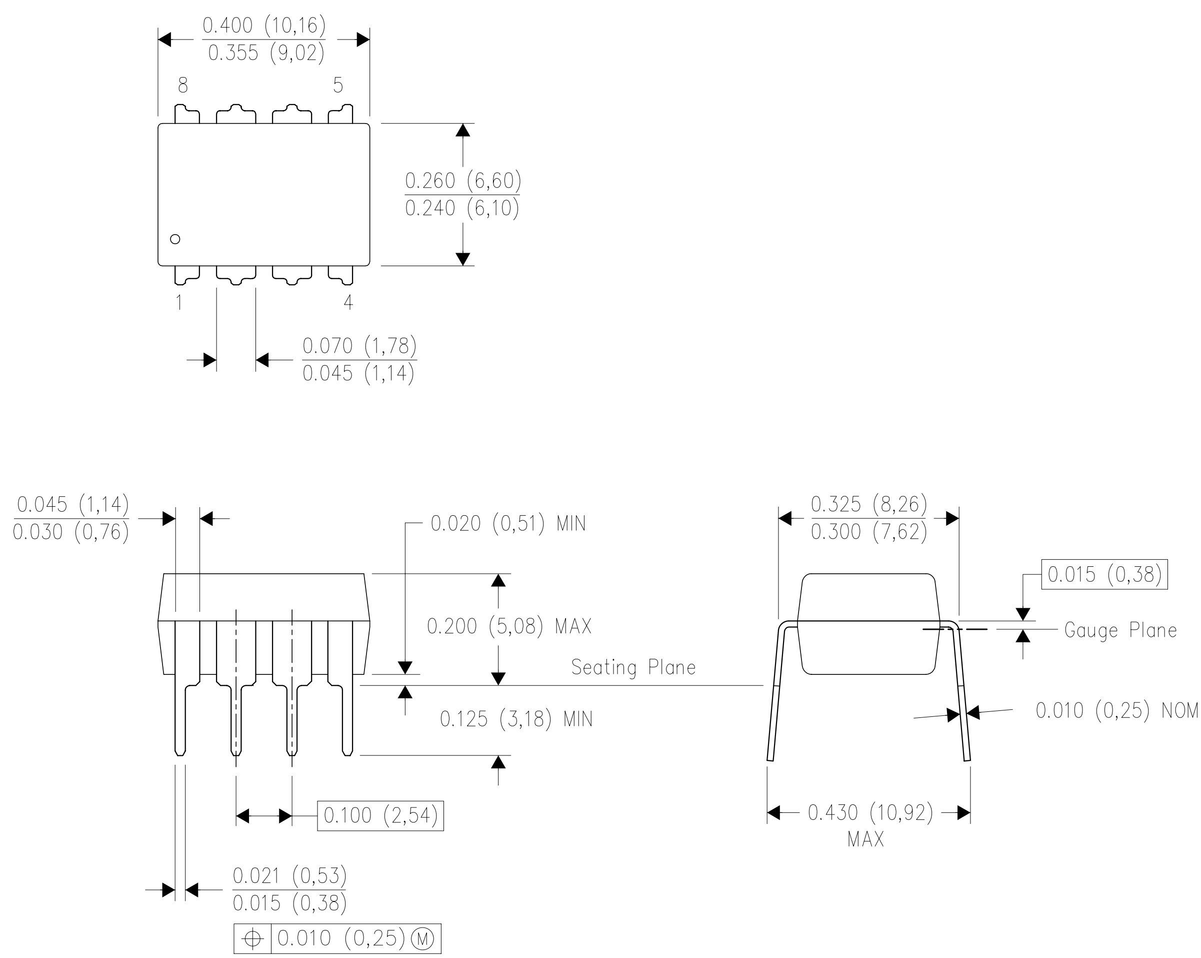
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

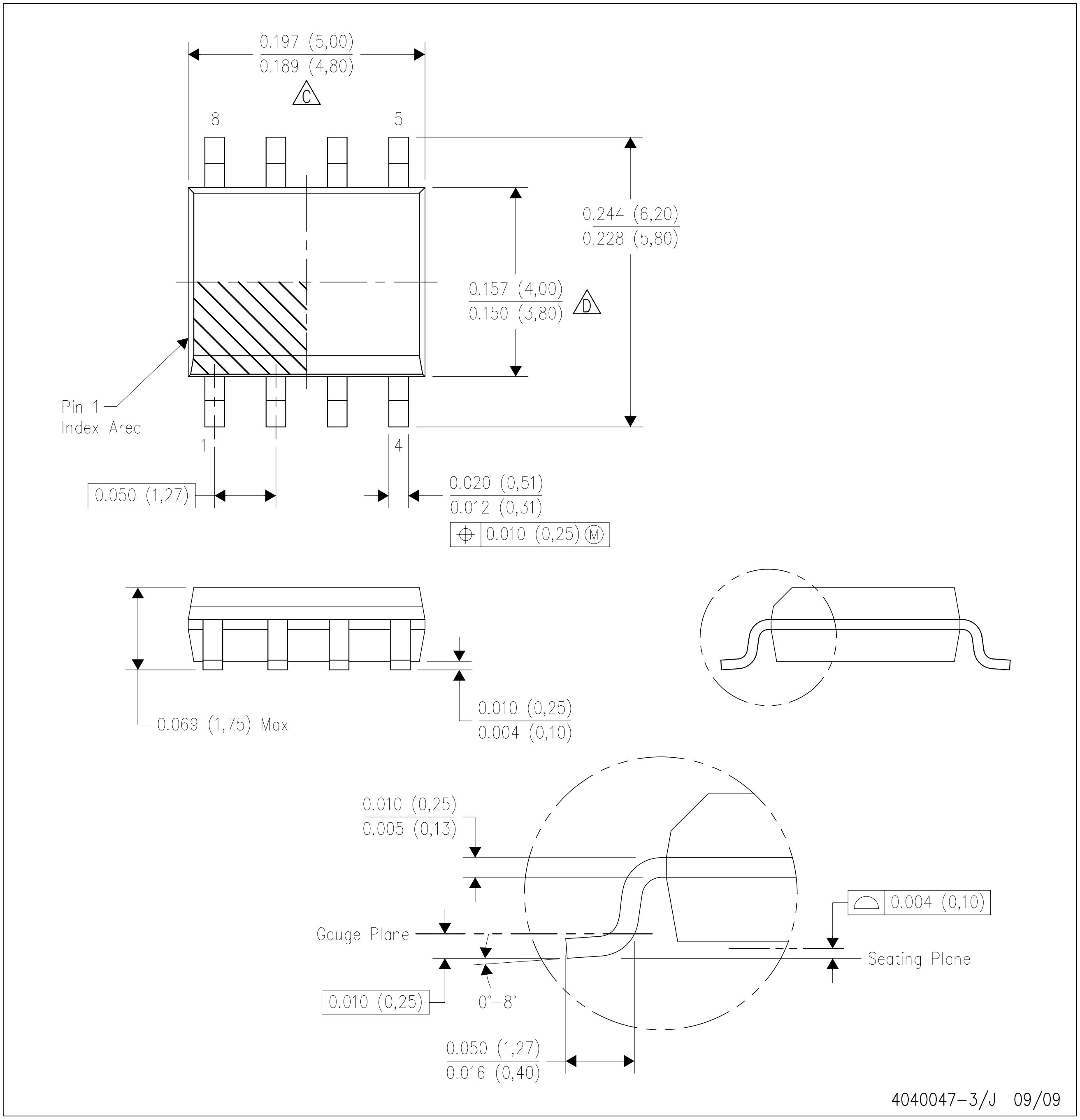
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



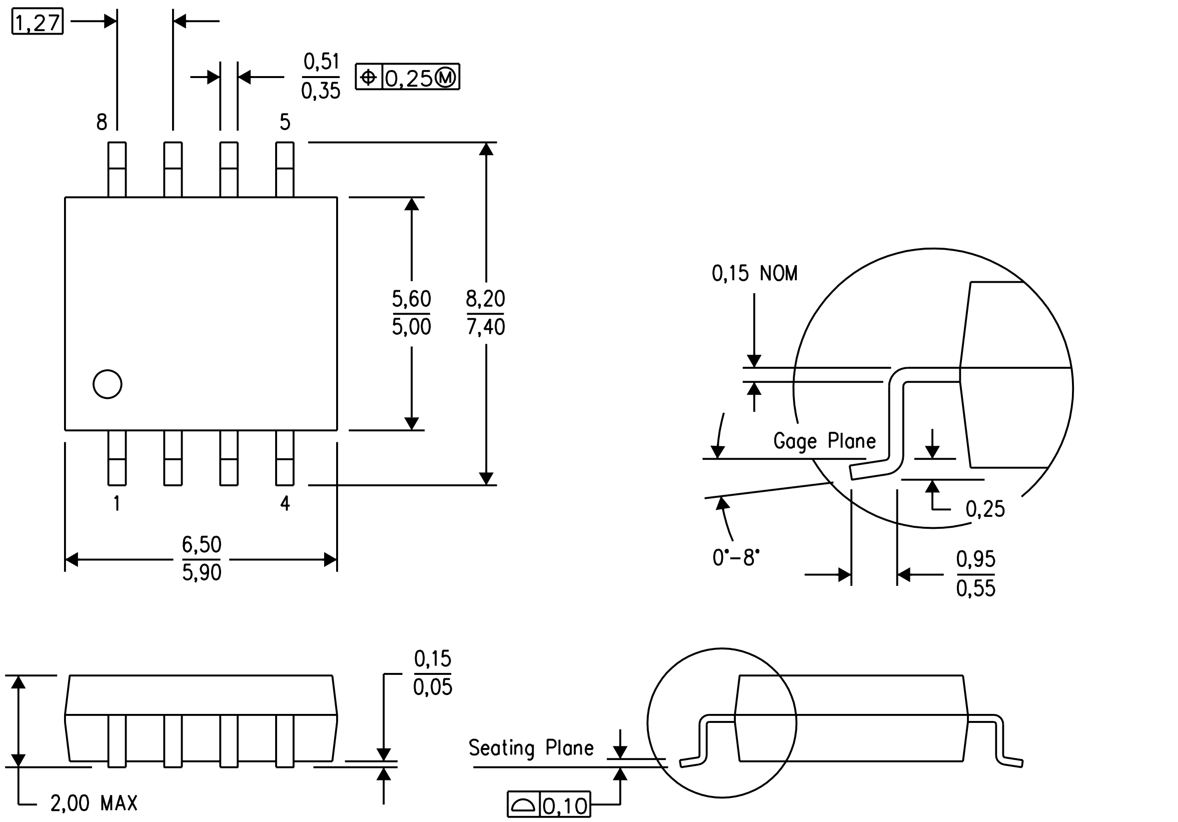
4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



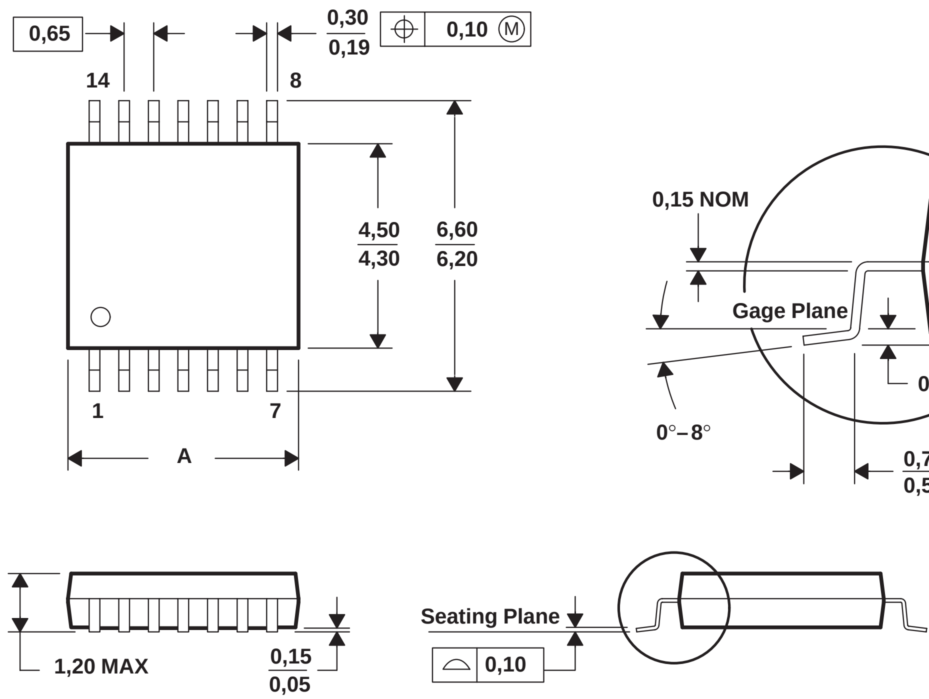
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153