DATA SHEET

BF998; BF998R
Silicon N-channel dual-gate MOS-FETs

Product specification
Supersedes data of April 1991
File under Discrete Semiconductors, SC07

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Philips Semiconductors

PHILIPS

Silicon N-channel dual-gate MOS-FETs — BF998; BF998R

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

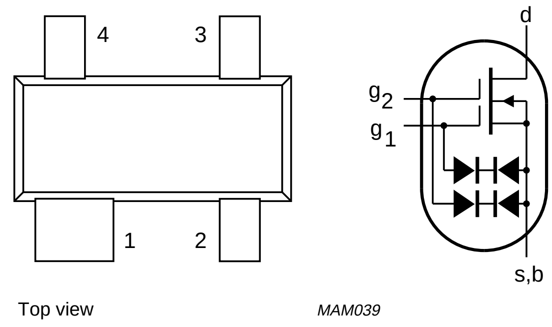
DESCRIPTION

Depletion type field effect transistor in a plastic microminiature SOT143 or SOT143R package with source and substrate interconnected. The transistors are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

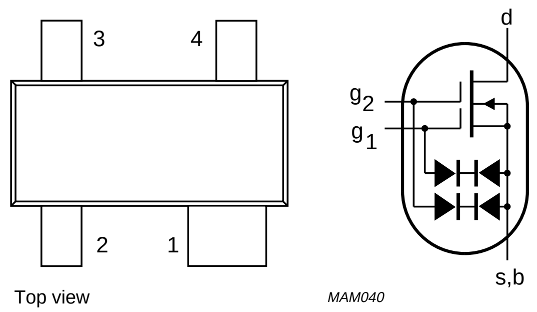
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MOp.

Fig.1 Simplified outline (SOT143) and symbol; BF998.



Marking code: MO$\bar{p}$.

Fig.2 Simplified outline (SOT143R) and symbol; BF998R.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
P_{tot}	total power dissipation		–	200	mW
$\|y_{fs}\|$	forward transfer admittance		24	–	mS
C_{ig1-s}	input capacitance at gate 1		2.1	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	25	–	fF
F	noise figure	f = 800 MHz	1	–	dB
T_j	operating junction temperature		–	150	°C

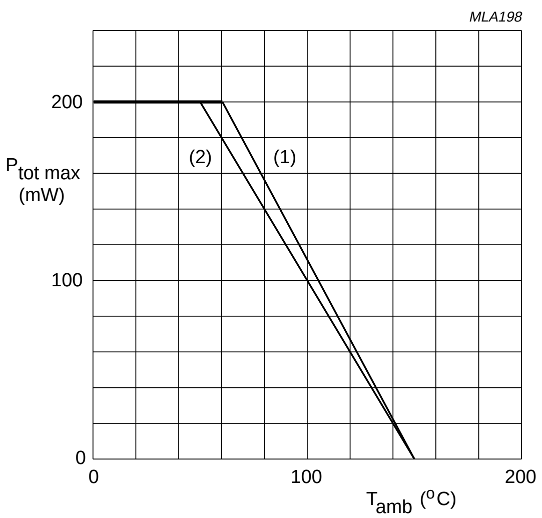
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
$\pm I_{G1}$	gate 1 current		–	10	mA
$\pm I_{G2}$	gate 2 current		–	10	mA
P_{tot}	total power dissipation; BF998	up to T_{amb} = 60 °C; see Fig.3; note 1	–	200	mW
		up to T_{amb} = 50 °C; see Fig.3; note 2	–	200	mW
P_{tot}	total power dissipation; BF998R	up to T_{amb} = 50 °C; see Fig.4; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Notes

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
2. Device mounted on a printed-circuit board.



(1) Ceramic substrate.
(2) Printed-circuit board.

Fig.3 Power derating curves; BF998.

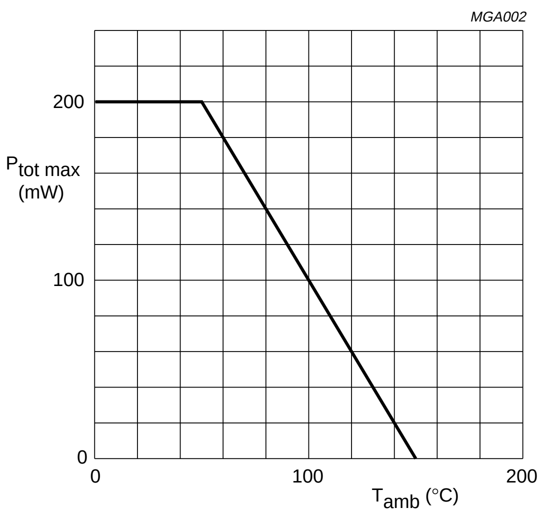


Fig.4 Power derating curve; BF998R.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air; BF998	note 1	460	K/W
		note 2	500	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air; BF998R	note 1	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
2. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}SS} = \pm 10$ mA	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}SS} = \pm 10$ mA	6	20	V
$-V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 8$ V; $I_D = 20$ μA	–	2.0	V
$-V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S} = 0$; $V_{DS} = 8$ V; $I_D = 20$ μA	–	1.5	V
I_{DSS}	drain-source current	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 8$ V; $V_{G1\text{-}S} = 0$; note 1	2	18	mA
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S} = \pm 5$ V	–	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S} = \pm 5$ V	–	50	nA

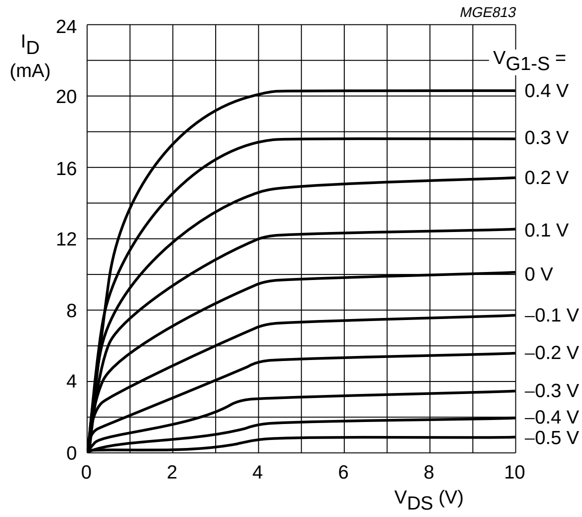
Note

1. Measured under pulse condition.

DYNAMIC CHARACTERISTICS

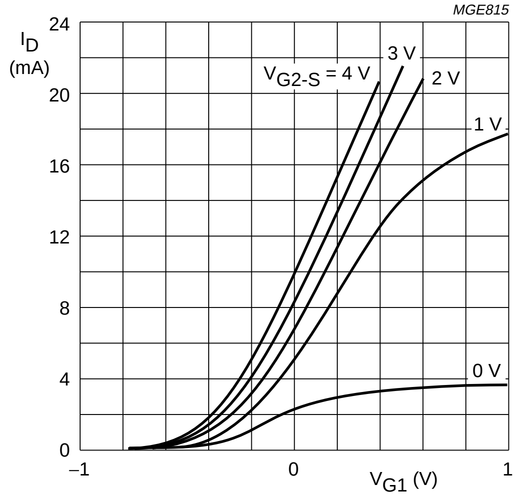
Common source; T_{amb} = 25 °C; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	f = 1 kHz	21	24	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.1	2.5	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	output capacitance	f = 1 MHz	–	1.05	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt}$	–	0.6	–	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{Sopt}$	–	1.0	–	dB



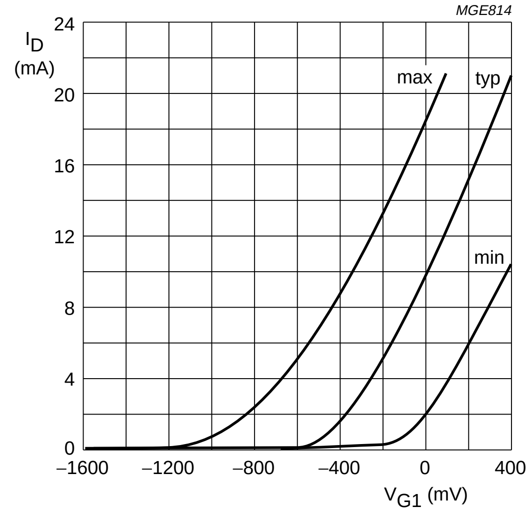
V_{G2-S} = 4 V; T_{amb} = 25 °C.

Fig.5 Output characteristics; typical values.



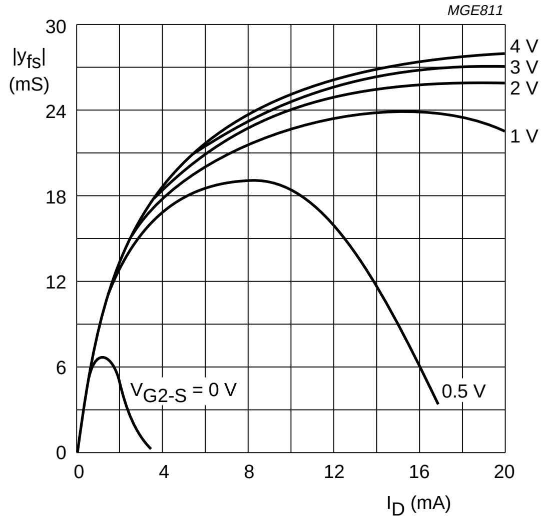
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.6 Transfer characteristics; typical values.



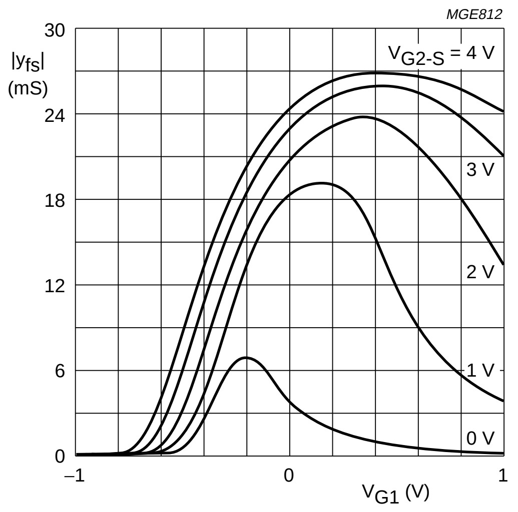
V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

Fig.7 Drain current as a function of gate 1 voltage; typical values.



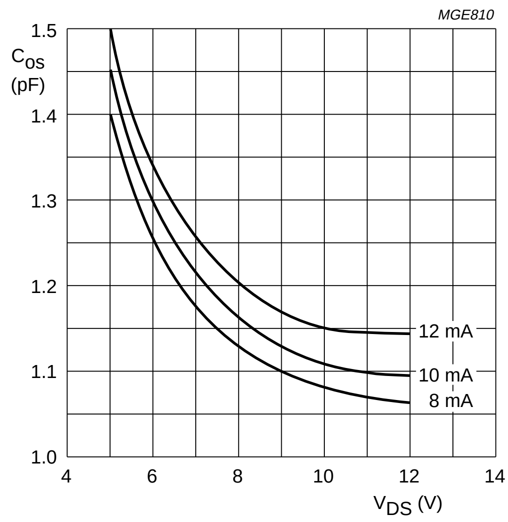
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



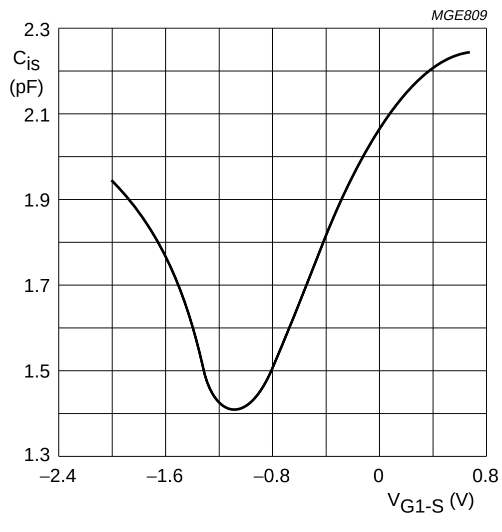
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.9 Forward transfer admittance as a function of gate 1 voltage; typical values.



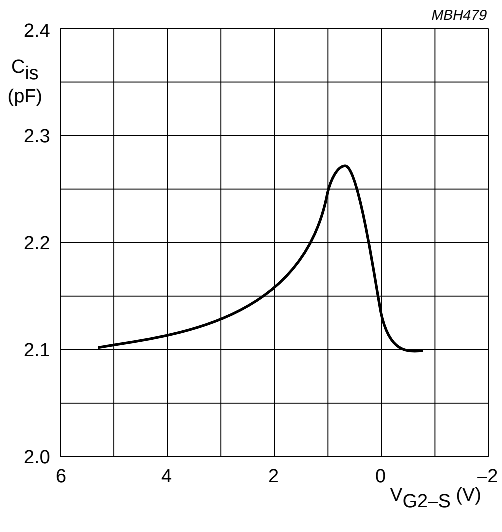
$V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.10 Output capacitance as a function of drain-source voltage; typical values.



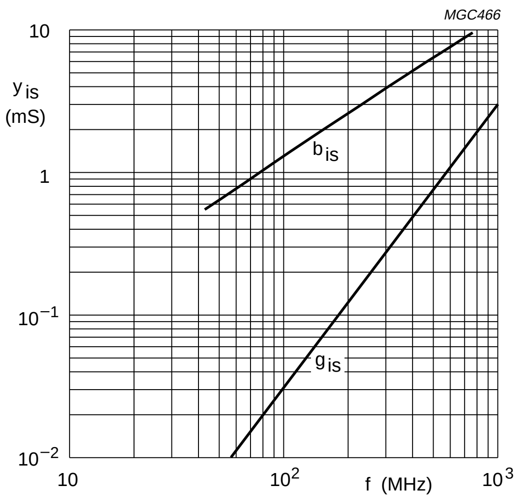
V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.11 Gate 1 input capacitance as a function of gate 1-source voltage; typical values.



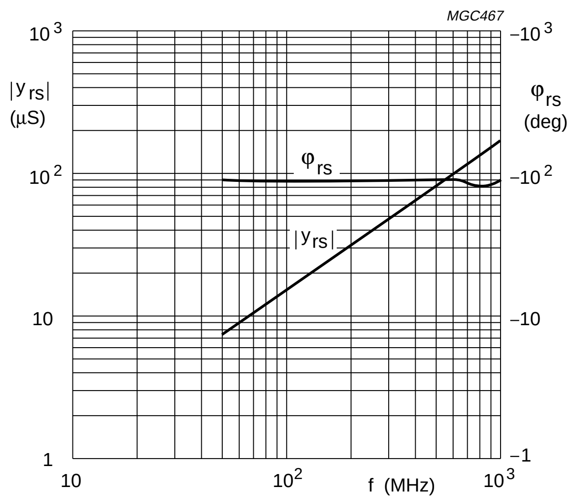
V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.12 Gate 1 input capacitance as a function of gate 2-source voltage; typical values.



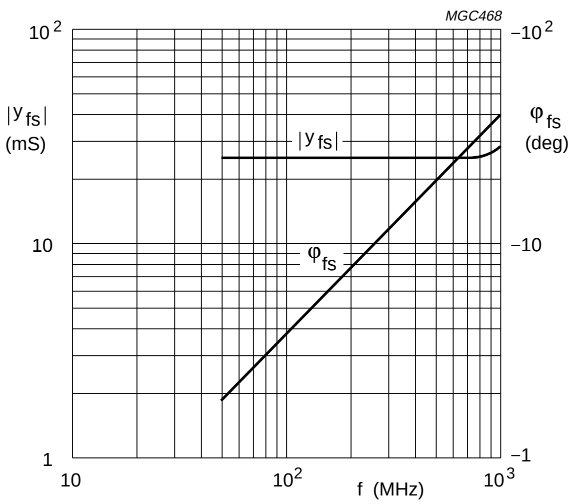
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.13 Input admittance as a function of the frequency; typical values.



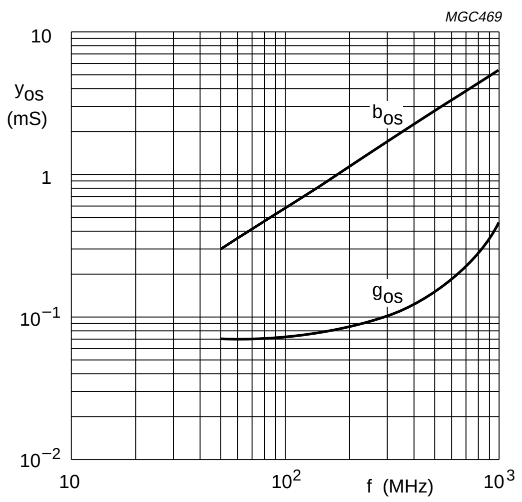
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.



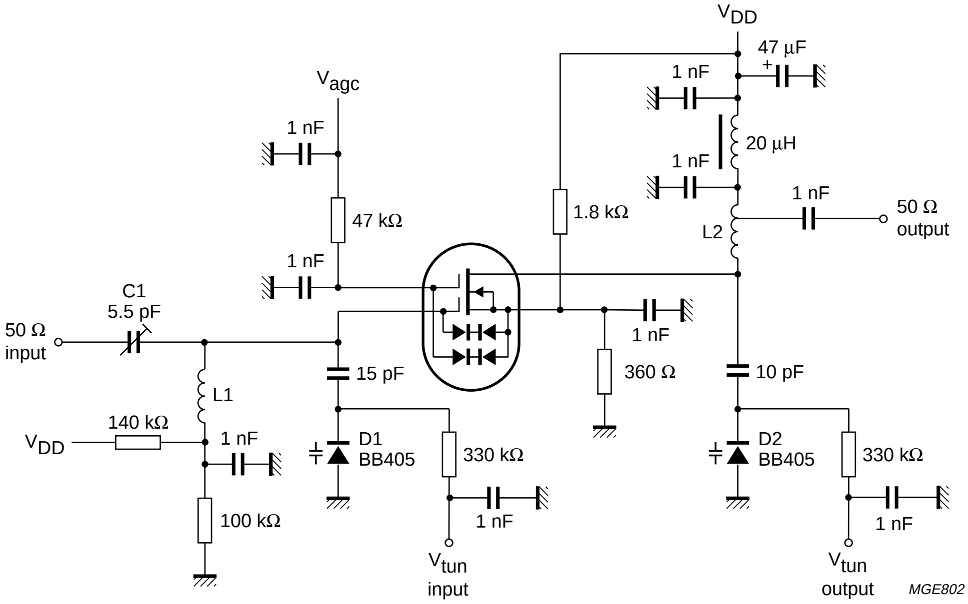
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.15 Forward transfer admittance and phase as a function of frequency; typical values.



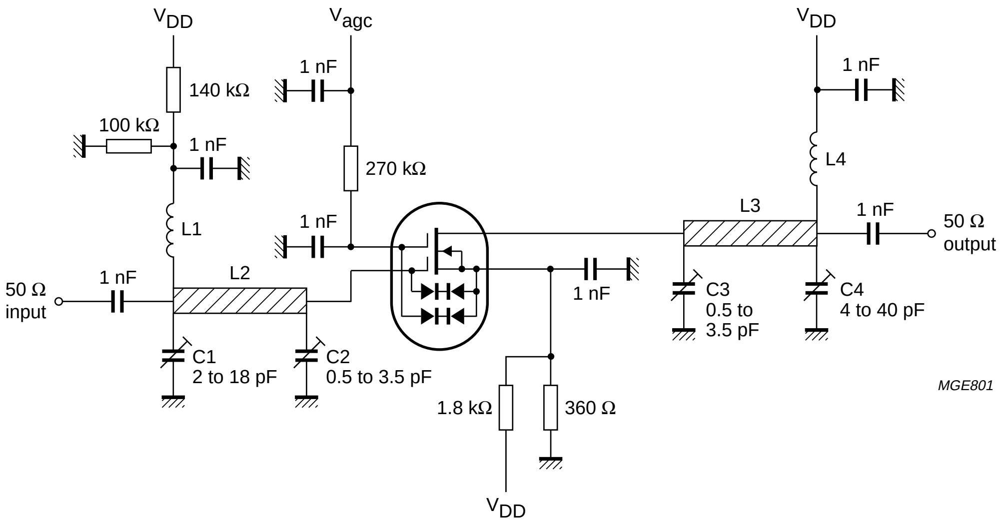
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.16 Output admittance as a function of the frequency; typical values.



V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.
L1 = 45 nH; 4 turns 0.8 mm copper wire, internal diameter 4 mm.
L2 = 160 nH; 3 turns 0.8 mm copper wire, internal diameter 8 mm.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS. C1 adjusted for G_S = 2 mS.

Fig.17 Gain control test circuit at f = 200 MHz.



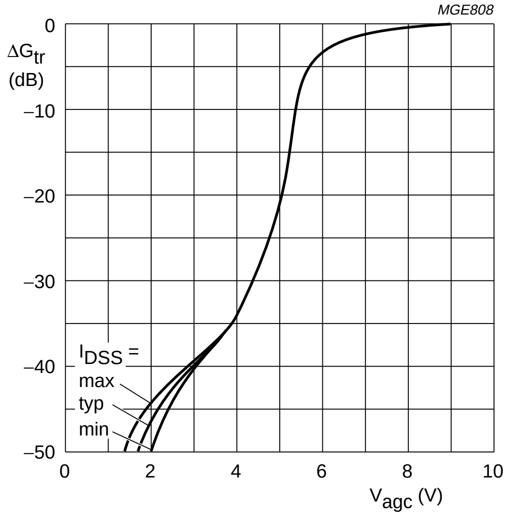
V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

L1 = L4 = 200 nH; 11 turns 0.5 mm copper wire, without spacing, internal diameter 3 mm.

L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.

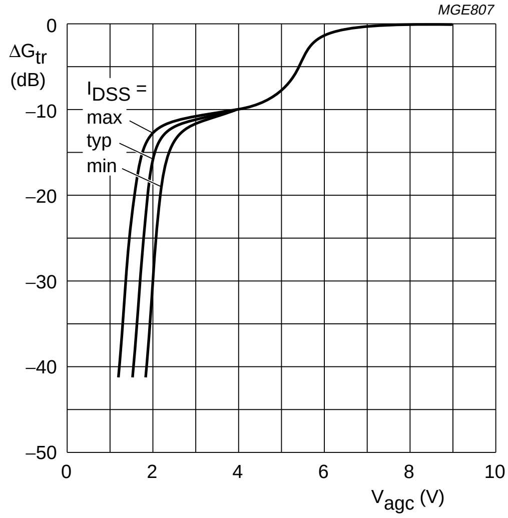
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.18 Gain control test circuit at f = 800 MHz.



V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

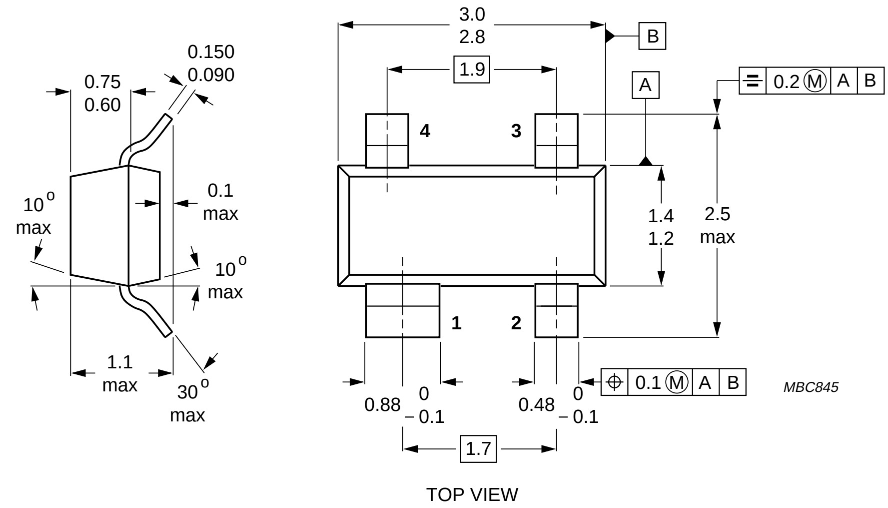
Fig.19 Automatic gain control characteristics measured in circuit of Fig.17.



V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

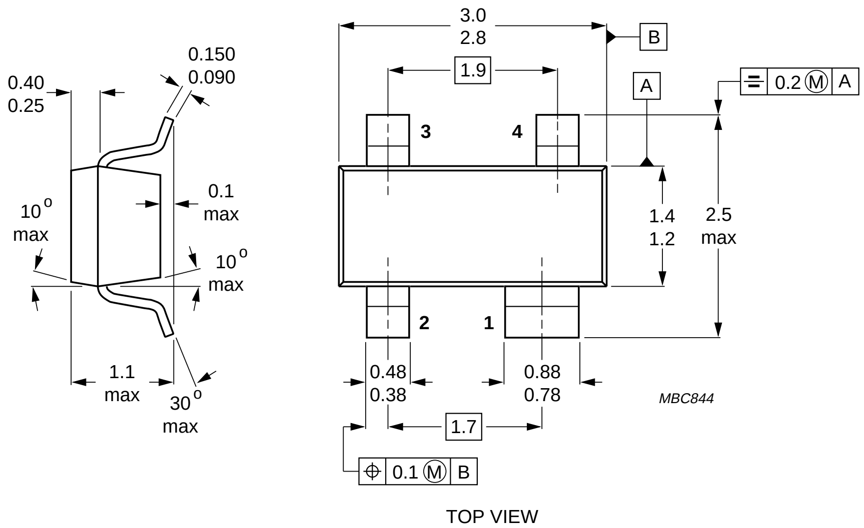
Fig.20 Automatic gain control characteristics measured in circuit of Fig.18.

PACKAGE OUTLINES



Dimensions in mm.

Fig.21 SOT143.



Dimensions in mm.

Fig.22 SOT143R.

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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